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THESIS

MEASURED PERFORMANCE OF A DELAY LOCK TRACKING LOOP
WHEN NOISE POWER EXCEEDS SIGNAL POWER

by

Joseph Michael Hanratty

March 1982

Thesis Advisor: G. A. Myers

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In the communications area there is a general interest in recovering signals below the noise level. In the military this interest translates to low-probability-intercept (LPI) and anti-jam (AJ) communications systems. The receiver improves the signal-to-noise ratio so data can be reliably recovered. This improvement is usually accomplished by matched filtering or by correlation.

In this report correlation is used as a post-detection processing technique to derive a synchronous reference. The system considered in this experiment can

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operate noncoherently by means of a delay lock tracking loop at signal-to-noise ratios as small as -5.0 to -7.1 dB. Futhermore, synchronization is achieved while the received signal is being modulated by data. No preamble or other type of synchronization is required.

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Measured Performance of a Delay Lock Tracking Loop When Noise Power Exceeds Signal Power

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requirements for the degree of

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In this report correlation is used as a post-detection processing technique to derive a synchronous reference. The system considered in this experiment can operate noncoherently by means of a delay lock tracking loop at signal-to-noise ratios as small as -5.0 to -7.1 dB. Futhermore, synchronization is achieved while the received signal is being modulated by data. No preamble or other type of synchronization is required.

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TABLE OF SYMBOLS

$b_r(t)$	m-sequence bandwidth
$d(t)$	transmitted data
$\hat{d}(t)$	recovered data
f_c	delay lock tracking loop filter bandwidth
f_d	frequency difference between transmitter's and receiver's data clocks
f_ℓ	frequency of receiver's data clock
f_r	frequency of transmitter's data clock
$m(t)$	m-sequence generated in transmitter
$m_e(t)$	receiver's early version of the received m-sequence
$m_\ell(t)$	receiver's late version of the received m-sequence
$m_p(t)$	receiver's punctual version of the received m-sequence
$m_r(t)$	m-sequence recovered by the receiver
$n(t)$	white Gaussian noise
$s(t)$	transmitter's transmitted signal
$v_e(t)$	loop's early correlation voltage
$v_\ell(t)$	loop's late correlation voltage
$v_p(t)$	receiver's punctual correlation voltage
$\hat{v}_d(t)$	initial version of the loop error voltage
$v_d(t)$	final version of the loop error voltage
G	loop gain
L	m-sequence code length
P_e	probability of error
$R_{mm}(t)$	m-sequence autocorrelation function

T chip interval (clock pulse interval)

τ phase offset between correlating m-sequences

I. INTRODUCTION

In the communications area there is a general interest in recovering signals which are below the noise level. In the military this interest translates to low-probability-of-intercept (LPI) and anti-jam (AJ) communications systems. The receiver improves the signal-to-noise ratio so data can be reliably recovered. This improvement is usually accomplished by matched filtering or by correlation.

This study considers using correlation as a post-detection processing technique to derive a synchronous reference. Of the various correlation techniques available, a delay lock tracking loop (DLTL) is used. In this research we ask the question: What is the effect of this DLTL on the receiver's operation? This study investigates experimentally the performance of a DLTL at input signal-to-noise ratios (SNR) of various levels. The results we find are that reliable data is recovered at a SNR as small as -5 to -7.1 dB. Furthermore, the circuit developed allows for synchronization to occur while the received signal is being modulated by data. No preamble or other type of synchronization is required.

Chapter II of this report explains how the DLTL acquires synchronization, how it tracks, and how noise affects its

operation. In Chapter III a description of the experimental system and its operation is given. Finally, Chapter IV presents the results of this study and their importance.

II. DESCRIPTION OF THE RESEARCH

A. OBJECTIVES

A primary objective of this study is to evaluate the effectiveness of a DLTL as a means for synchronizing a direct sequence spread spectrum communications system. In this study, a noncoherent amplitude modulation (AM) communications receiver is made to operate completely asynchronously by means of a DLTL.

In achieving the above objective, this study has a secondary objective of evaluating the performance of this DLTL under conditions of low signal-to-noise ratio. This evaluation involves observing and measuring the effects of various loop parameters (loop bandwidth and loop gain) under varying operating conditions (relative frequency offset and SNR).

B. THE DIRECT SEQUENCE SPREAD SPECTRUM SYSTEM

The system considered here is a direct sequence spread spectrum communications system. Block diagrams of the transmitter and receiver are shown in Figures 2.1 and 2.2, respectively.

In the transmitter a 1023 chip long m-sequence is generated by a ten stage feedback shift register (FSR). Data modulation of each m-sequence is accomplished by modulo-two

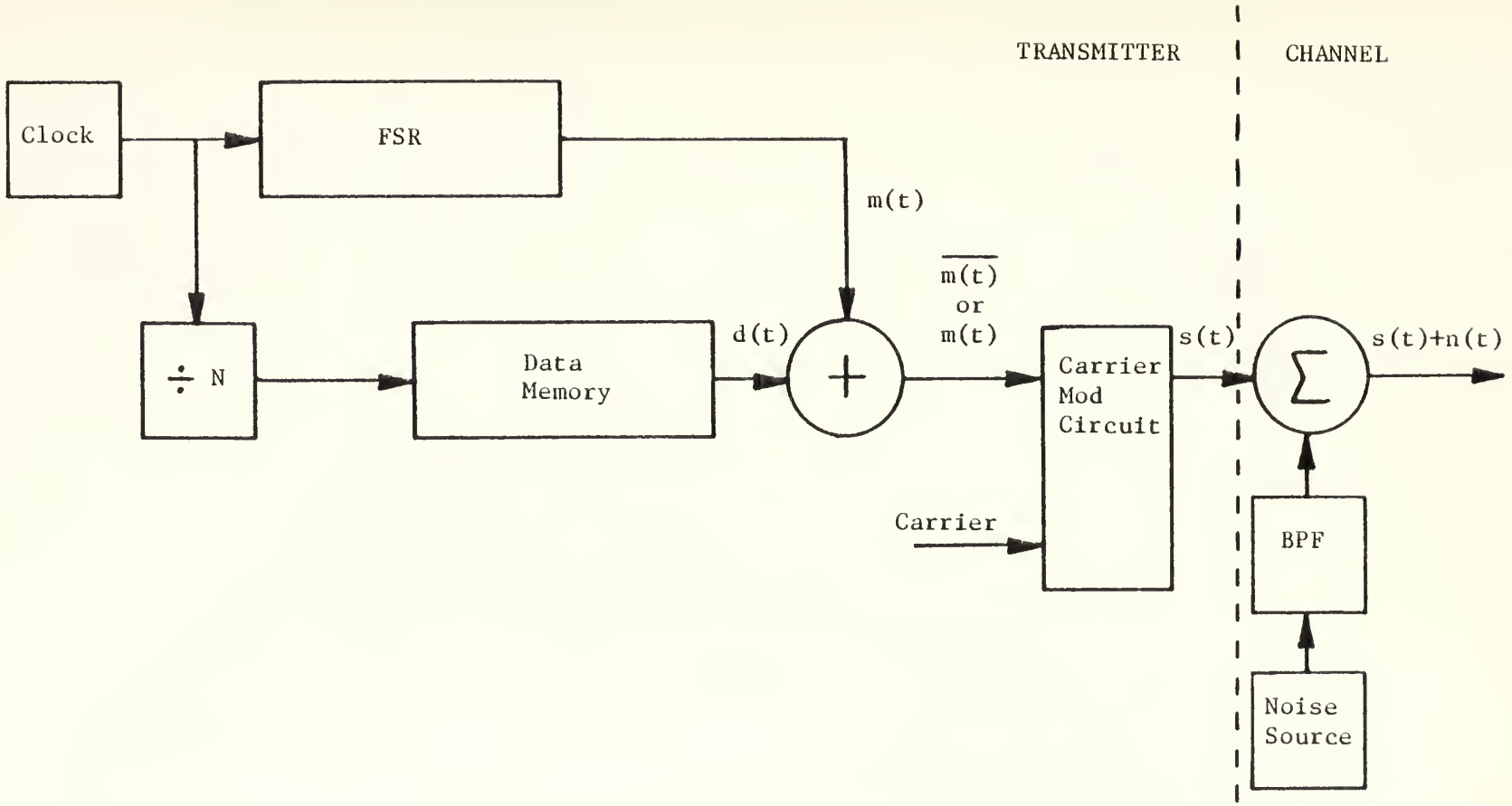


FIGURE 2.1 TRANSMITTER AND CHANNEL BLOCK DIAGRAM

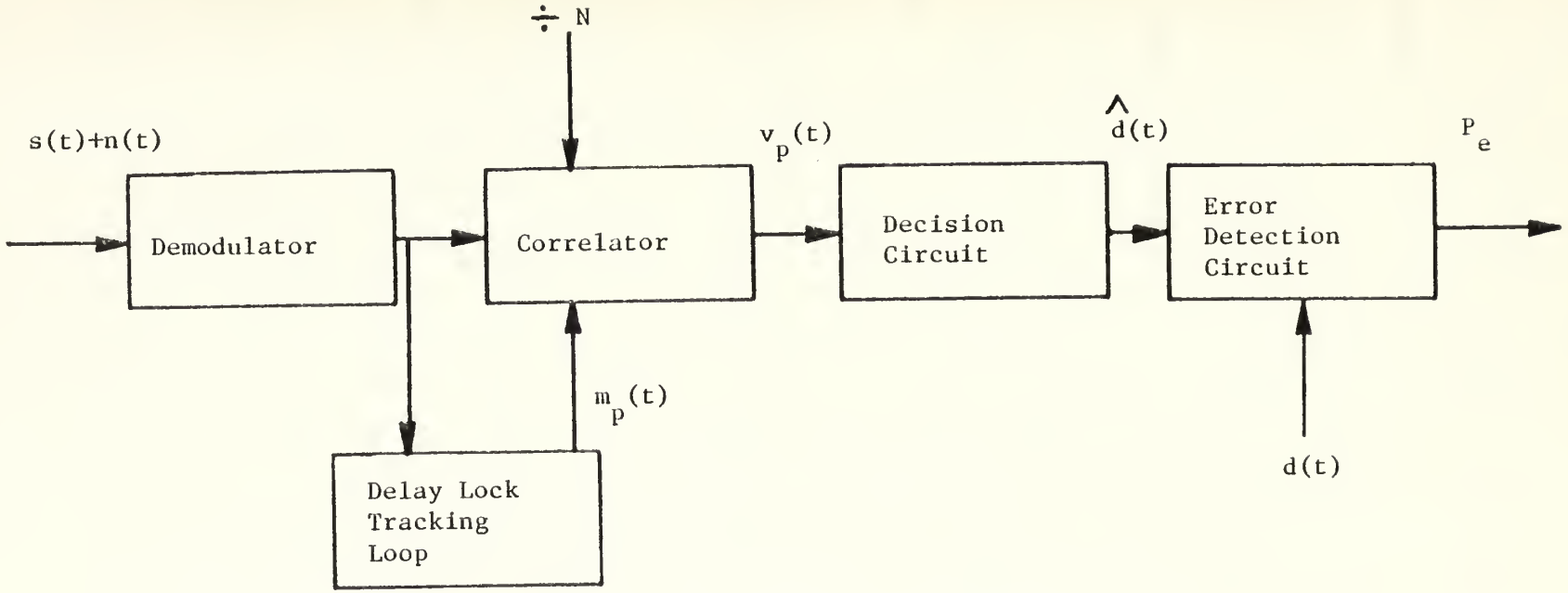
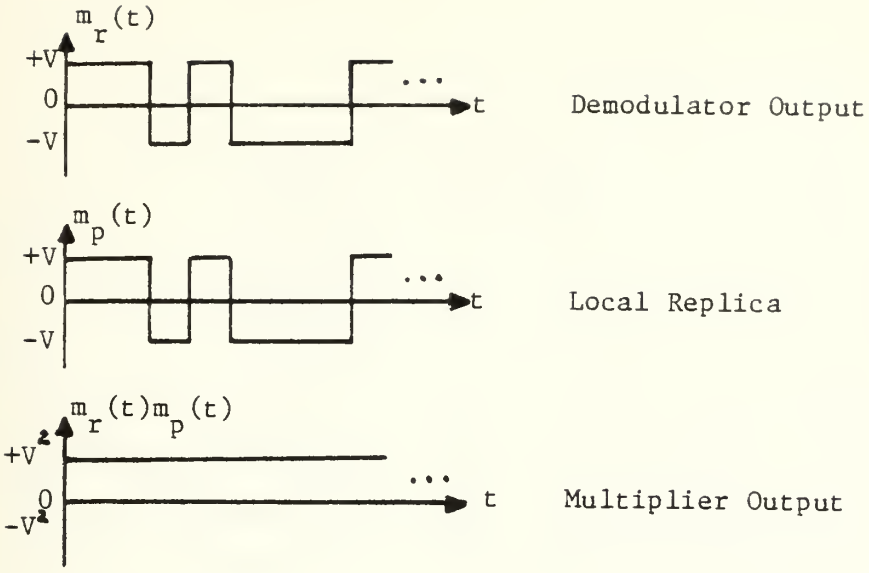


FIGURE 2.2 RECEIVER BLOCK DIAGRAM

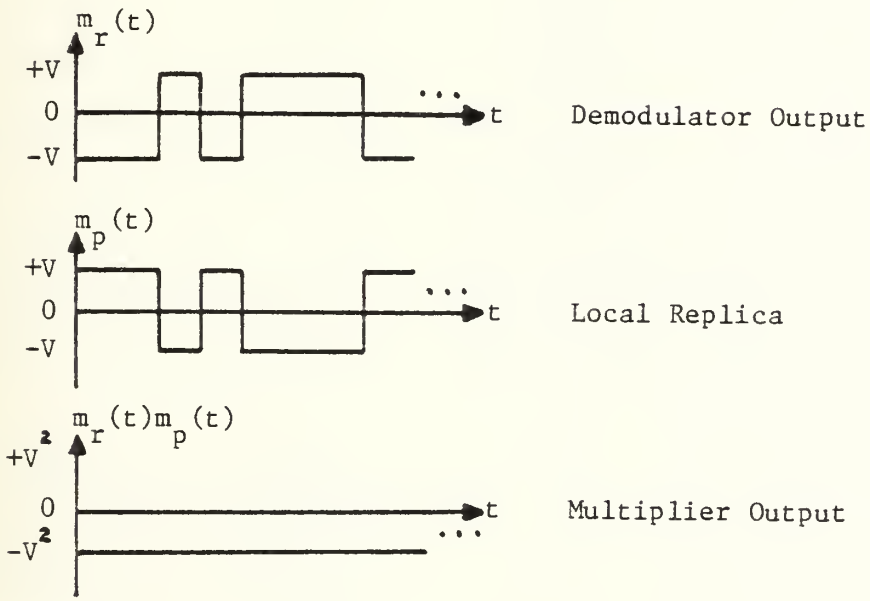
summing m(t) with the data d(t). The resulting m-sequence, m(t), or its complement, $\overline{m(t)}$, is used to "on-off" amplitude modulate a sinusoidal carrier. The resulting signal s(t) is transmitted.

Noise n(t) is added to the transmitted signal to simulate the system channel. This noise is band limited to simulate the amount of noise which would be passed through the tuned IF amplifier of a superheterodyne receiver. The input to the receiver is then s(t)+n(t).

In the receiver three conditions must be met prior to data recovery. (1) The received m-sequence $m_r(t)$ must be formed. After initial filtering and amplification by the receiver front end, the received signal s(t)+ n(t) is envelope detected to obtain $m_r(t)$ imbedded in noise. (2) The recovered noisy m-sequence must be correlated with a local replica $m_p(t)$ to form constant voltage levels which represent the data. Figure 2.3 shows this multiplication operation when there is no noise and the resulting voltage levels which represent reception of a data "1" $[m_r(t)]$ and a data "0" $[\overline{m_r(t)}]$. (3) For best recovery of data, $m_r(t)$ and $m_p(t)$ must be in phase. Figure 2.4 shows that if $m_r(t)$ is offset in time (phase shifted) from $m_p(t)$, then a smaller constant voltage representing the data occurs and our ability to decide on the data in the presence of noise diminishes. To achieve this best recovery of data, a DLTL is



(a) "1" Transmitted



(b) "0" Transmitted

FIGURE 2.3 CORRELATOR MULTIPLIER OUTPUT

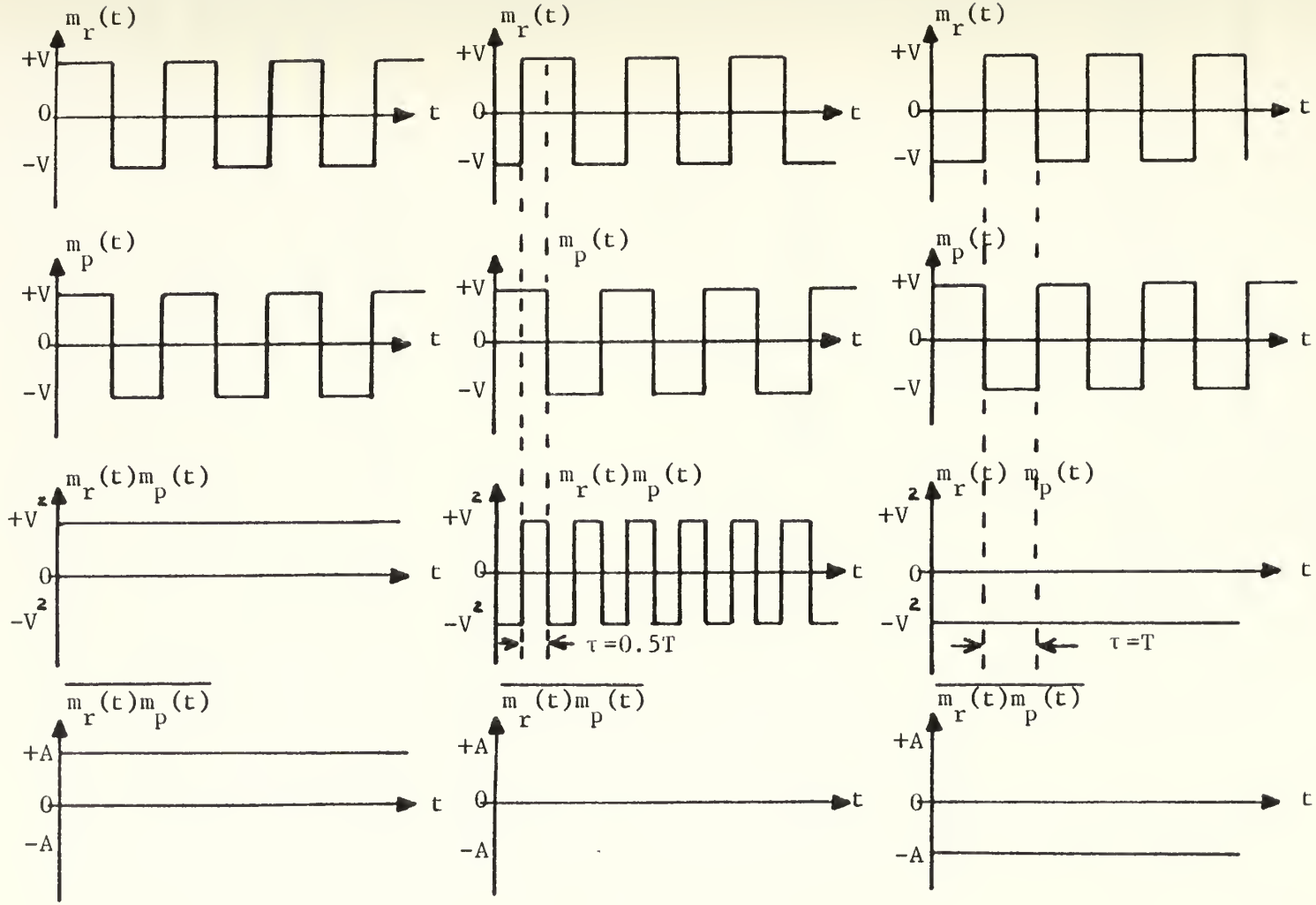


FIGURE 2.4 EFFECTS OF PHASE OFFSET ON CORRELATOR OUTPUT VOLTAGES

used to generate the local replica $m_p(t)$ which is synchronized in frequency and phase with $m_r(t)$.

Correlation of $m_r(t)$ with $m_p(t)$ produces voltage levels representative of the original data. The correlation operation is accomplished by first forming the product of $m_r(t)$ and $m_p(t)$, and then averaging this product. The correlation operation can be modeled as shown in Figure 2.5.

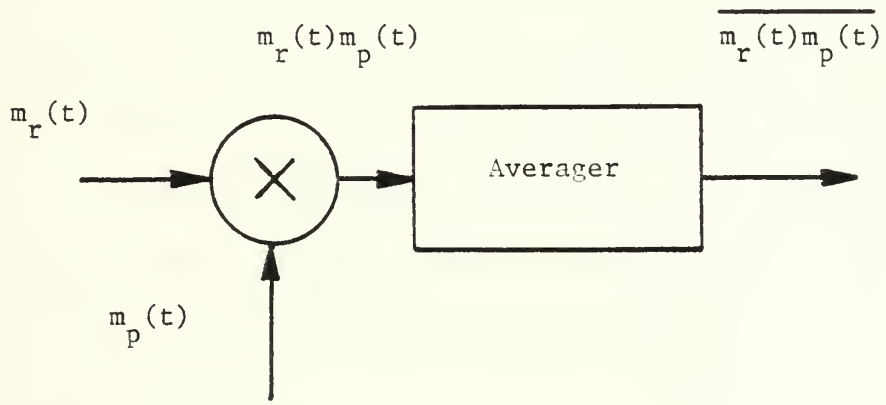


FIGURE 2.5 CORRELATOR MODEL

The receiver's decision circuit converts these correlator voltage levels to binary estimates of the original data. Finally, an error detection circuit compares this binary estimate with the data actually transmitted to determine P_e the rate of error occurrence. Montoya [Ref.1] provides a detailed discussion of the operation of each system component shown in Figures 2.1 and 2.2.

C. DELAY LOCK TRACKING LOOP THEORY OF OPERATION

Data is recovered in the receiver by correlating $m_r(t)$ with its locally produced replica $m_p(t)$. Best recovery of data occurs when these two signals are synchronized in frequency and in phase. When $m_r(t)$ and $m_p(t)$ are in phase, then the correlator output is a maximum as shown in Figure 2.4 and we decide a data "1" or "0" was transmitted (Figure 2.3). But good decisions require the received and local sequences to remain in phase throughout the entire data bit interval (one period of the m-sequence). The DLTL provides this synchronization by appropriately using voltages like those in Figure 2.3 to adjust the output frequency (and phase) of a voltage-controlled oscillator (VCO) placed in the feedback loop. The VCO output becomes the receiver clock which in this manner provides timing for $m_p(t)$ exactly like that of $m_r(t)$.

1. Basic Operation

Synchronization is achieved by an early minus late gate technique. As show in Figure 2.6, the loop's synchronization process can be divided into three operational blocks: (1) m-sequence generation, (2) correlation, and (3) summation. In the first block, the loop generates three replicas of the received m-sequence. Two of these replicas, $m_e(t)$ and $m_\ell(t)$, are used in the second block for simultaneous correlation with the received m-sequence $m_r(t)$. The resulting correlation voltages are

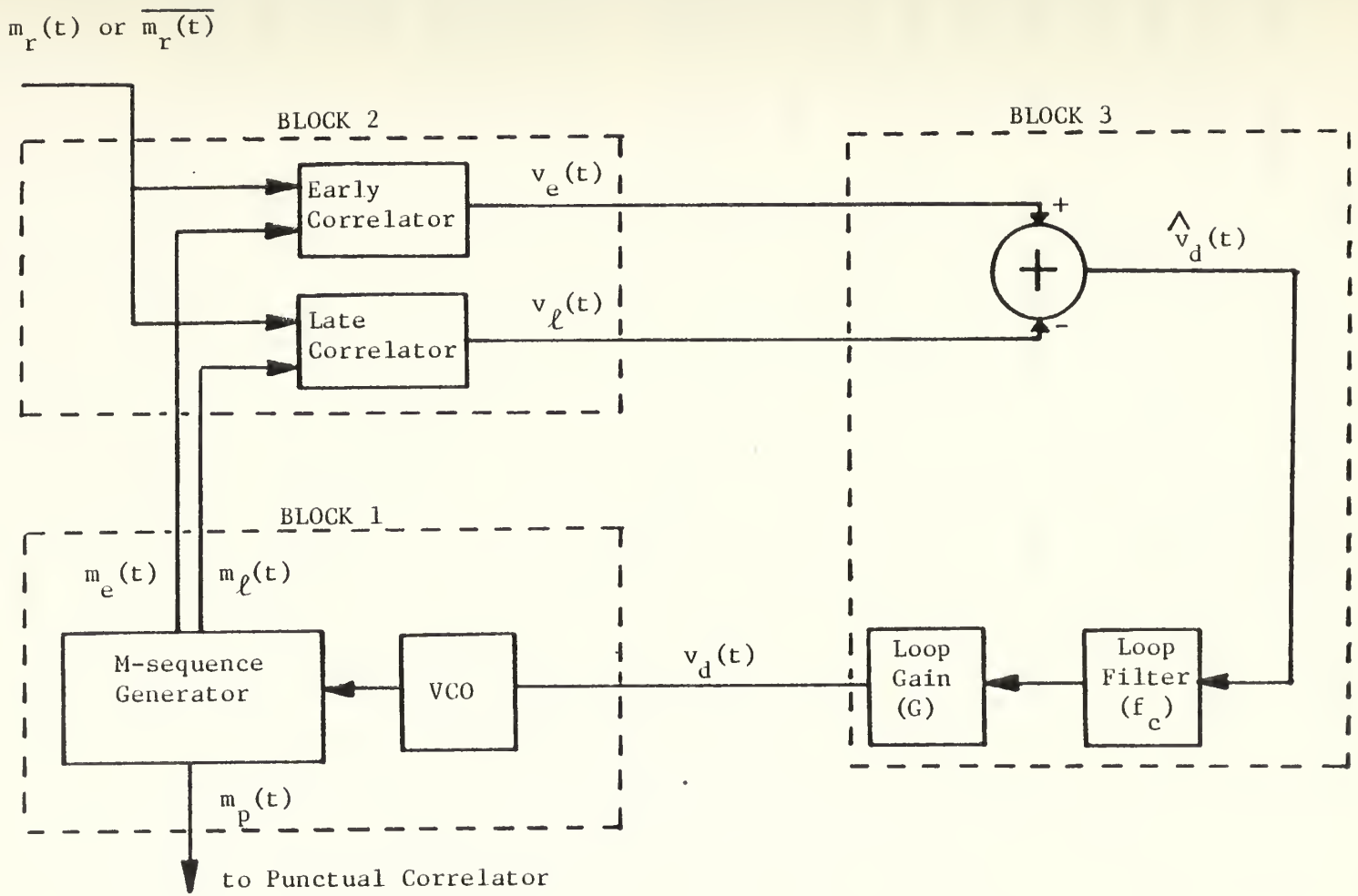


FIGURE 2.6 DELAY LOCK TRACKING LOOP BLOCK DIAGRAM

summed in the third block to form the loop error voltage, $v_d(t)$. This voltage is fed back to the VCO in the first block to control the rate of local m-sequence generation.

In the first operational block, the loop's clock (VCO) steps a FSR which is identical to the one found in the transmitter so that the m-sequences generated locally are identical in form to the one received. Derived from this FSR are three m-sequences: early, punctual, and late. They are identical but displaced from each other in time by one chip interval T. The early and late m-sequences are separated in time by two chip intervals (two clock pulse intervals). The punctual m-sequence $m_p(t)$ is applied to the punctual correlator for correlation with $m_r(t)$ to recover data. The early and late m-sequences, $m_e(t)$ and $m_\ell(t)$, are applied to their respective loop correlators in block two.

In block two, $m_e(t)$ and $m_\ell(t)$ correlate with $m_r(t)$ to produce components of the loop error voltage $v_d(t)$. Depending on the initial phase difference between the received and local m-sequences, $m_r(t)$ may correlate first early then late or vice-versa. If $m_r(t)$ correlates first early then late, then the outputs of the loop correlators become as shown in Figure 2.7. Here, $v_e(t)$ and $v_\ell(t)$ are the autocorrelation functions of the early and late m-sequences.

These correlator outputs are applied to the differential amplifier in block 3 where the initial version $v_d(t)$ of the loop error voltage is formed. This difference voltage

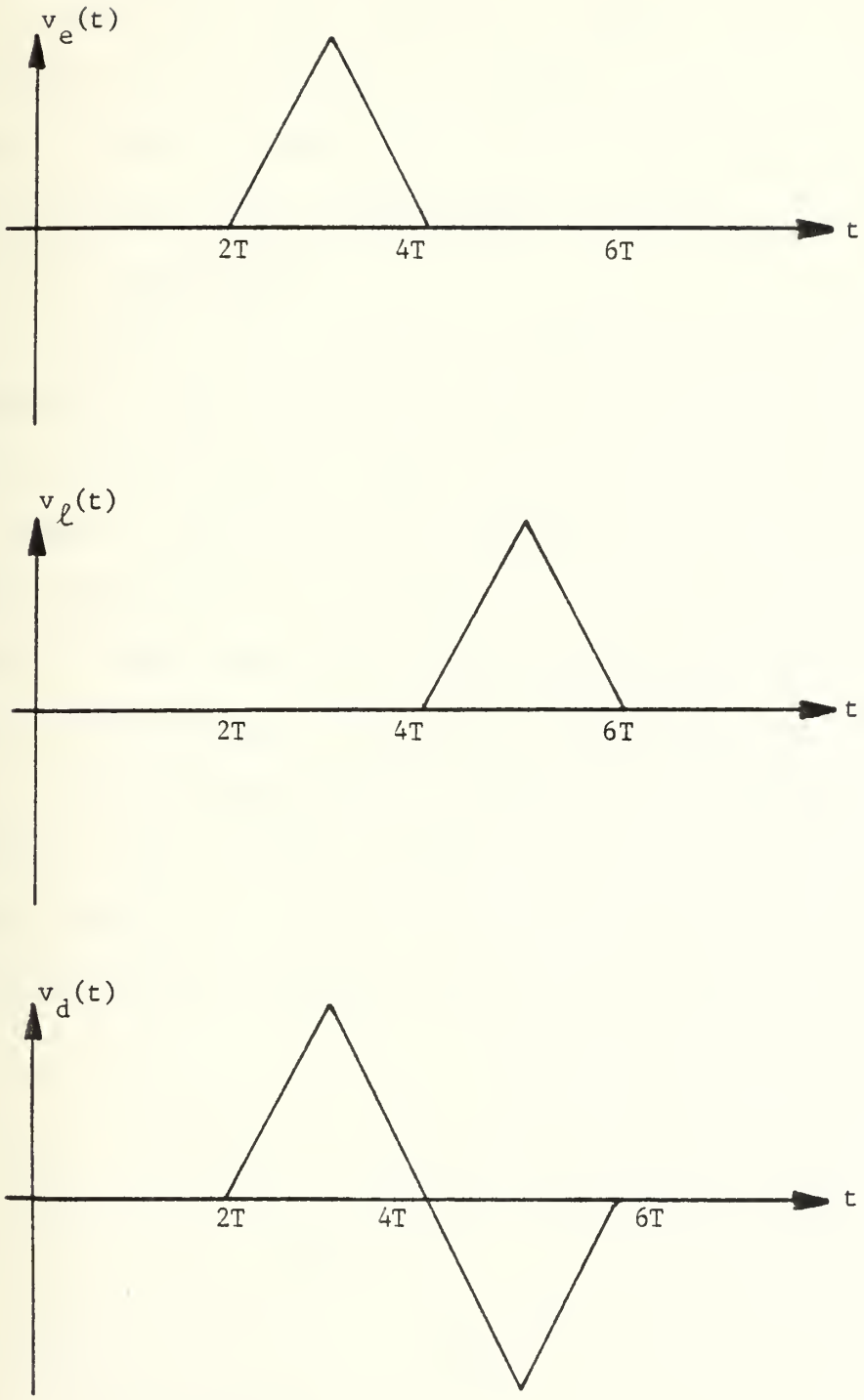


FIGURE 2.7 LOOP ERROR VOLTAGE FORMATION

(early- minus-late) is amplified and filtered to form the voltage-controlled oscillator (VCO) control voltage. Figure 2.7 shows this final version. Positive and negative error voltages $v_d(t)$ slow down or speed up the clock (VCO output) which, in turn, change the relative passing rate between the received and local m-sequences.

2. Acquisition

When the loop is operating in the non-lock condition, the received m-sequence and the local m-sequence pass by each other at some relative passing rate f_d. Here, f_d equals the difference between the frequency f_ℓ of the local clock and the frequency f_r of the received clock. The loop can enter the lock condition whenever it experiences an early then late or a late then early correlation with $m_r(t)$.

To investigate the dynamics of acquisition, it is helpful to view the m-sequences as they pass one another. See Figure 2.8 where the state of the FSR output is represented by a binary number rather than a voltage level.

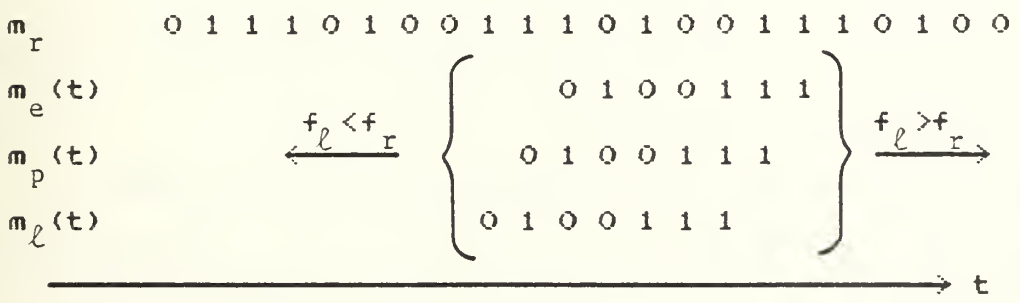


FIGURE 2.8 PASSING M-SEQUENCES

When $f_\ell > f_r$, the three local m-sequences move to the right with respect to the received m-sequence. Here, early correlation is followed by late correlation and the loop error voltage forms as shown in Figure 2.9. During lock the loop stablizes somewhere in the vicinity of point P_1 , a positive voltage necessary to force the VCO to slow down and follow f_r . Note that just prior to entering the lock condition a loop error voltage peak causes f_ℓ to become slower than f_r . This slow down just prior to lock simply moves the two m-sequences into alignment slower. A similar analysis can be made for the case where $f_\ell < f_r$. Here, early correlation follows late correlation and the appropriate loop error voltage forms as shown in Figure 2.9.

Note that in both cases the early correlation voltage $v_e(t)$ is always positive and the late correlation voltage $v_\ell(t)$ is always negative. This outcome is necessary assuming the VCO has a voltage-to-frequency chartacteristic of negative slope as shown in Figure 2.9. The opposite is also true. For a positive voltage-to-frequency characteristic, it is necessary that $v_e(t)$ be negative and $v_\ell(t)$ be positive. Any other combination will not allow the loop to lock.

There are two loop parameters which can be adjusted; loop bandwidth f_c and loop gain G. The loop bandwidth f_c is primarily determined by the bandwidth common to the correlator filters and the loop filter. It is shown in Appendix A

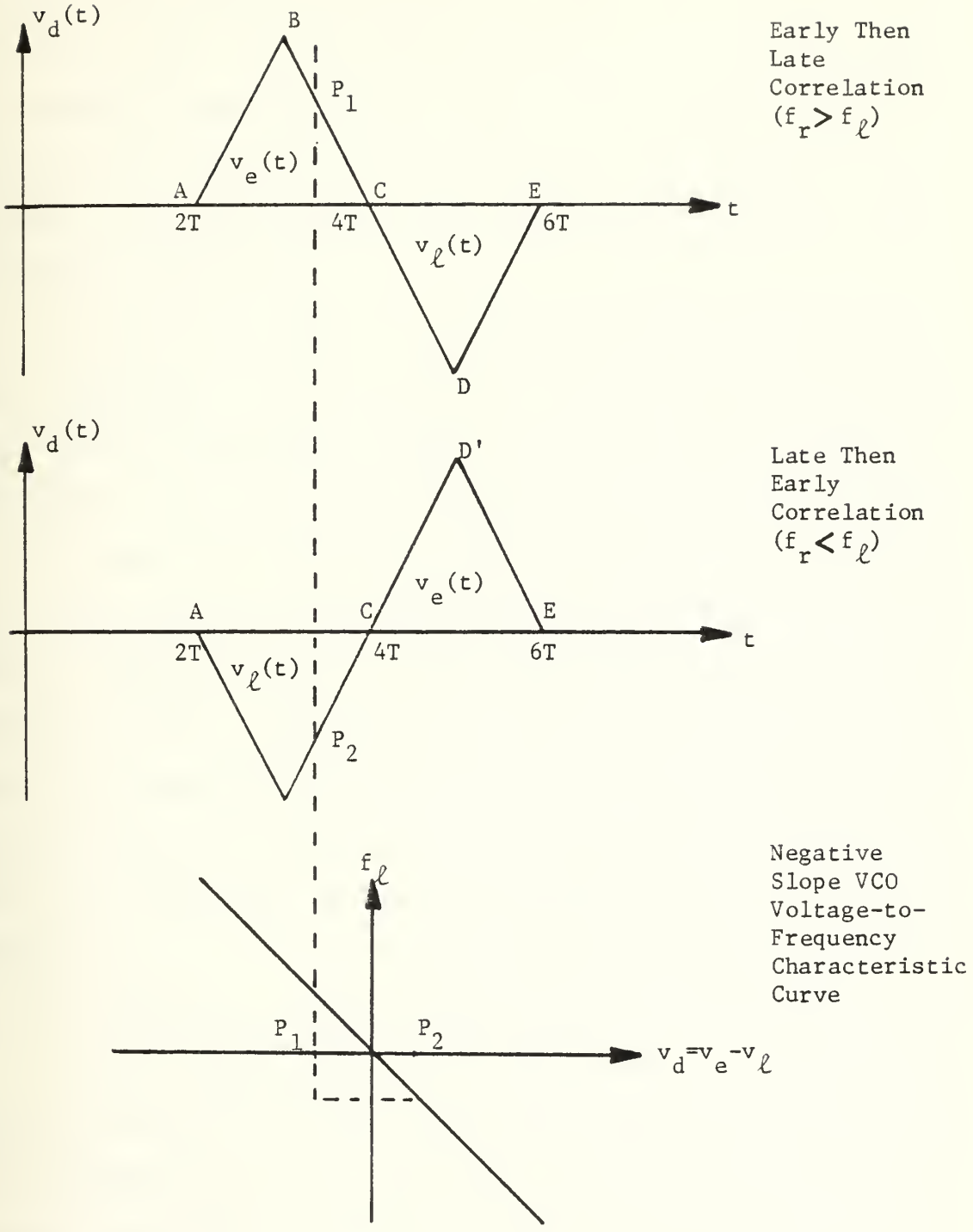


FIGURE 2.9 LOOP ERROR VOLTAGE CHARACTERISTICS

that a given relative passing rate f_d produces a loop error voltage with bandwidth equal to f_d. So, for acquisition the effective loop bandwidth must be equal to or greater than the greatest expected capture rate. Thus, loop filters are designed to filter out as much noise as possible while allowing only the appropriate loop error voltage to affect the loop's operation.

The loop gain G is determined by a simple voltage gain adjustment within the loop. For acquisition the loop gain must be adjusted in proper combination with the loop bandwidth. Too little gain prevents the loop from responding at all, and too much gain causes the loop to be unstable. Also, the loop gain affects the loop bandwidth. Spilker [Ref.2] shows that for a linearized model of the loop, a change in the loop gain directly affects the overall effective bandwidth of the loop. Thus, the loop bandwidth and gain affect the loop error voltage frequency components and the loop gain affects the magnitude of this error voltage.

3. Tracking

Once acquisition is achieved, the loop forces the VCO to follow or track the received m-sequence by supplying the appropriate error voltage. Tracking occurs over a certain loop error voltage range for a given loop bandwidth and gain. Shown in Figure 2.9 are the loop error voltages which are generated during the two possible capture

situations: $f_\ell < f_r$, and $f_\ell > f_r$, and the corresponding VCO voltage-to-frequency characteristic curve.

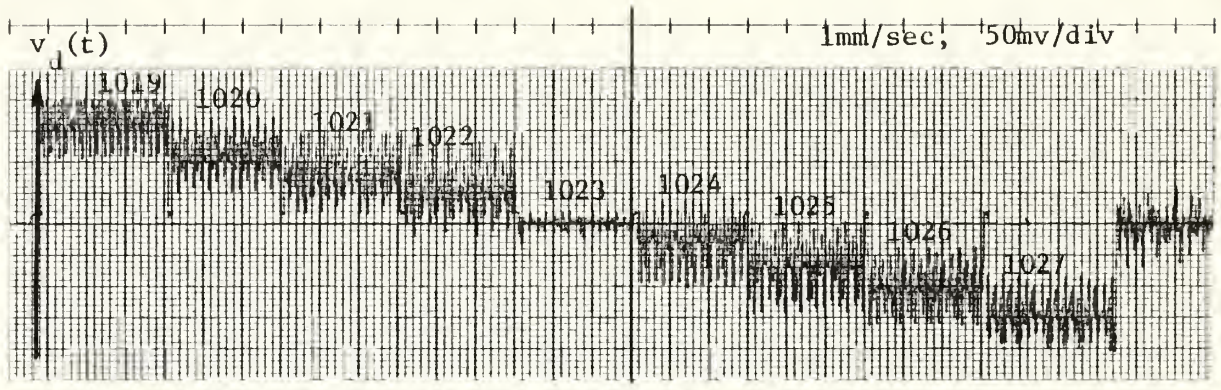
During acquisition a certain frequency difference establishes the initial operating point. Depending on which capture situation occurs, the loop will stablize somewhere along either line segment CB or CB'. The actual operating point depends on $f_d = f_r - f_\ell$. The greater f_d, the greater the voltage that is required to force the VCO to follow the incoming frequency, and the more the operating point displaces from C towards either B or B'. During tracking a change in either f_ℓ or f_r or both causes the the operating point to move anywhere along BCB'. The resulting negative voltage-to-frequency characteristic curve is shown in Figure 2.9. An operating point coincident with C means that f_ℓ and f_r are equal in both phase and frequency. At this point $m_r(t)$ exactly equals $m_p(t)$ and there is no phase offset. This condition causes a maximum output out of the punctual correlator as shown in Figure 2.4. A change in f_d shifts $m_r(t)$ in relation to $m_p(t)$ which causes the operating point to move closer to either B or B'. This phase shift causes a corresponding decrease in the punctual correlator's output (Figure 2.4). If the operating point reaches point B or B', the phase offset reaches a maximum, the punctual correlator's output reaches a minimum and chances are maximized for noise to move the operating point over to the unstable side of the loop error voltage (BA or B'A) where synchronization is lost.

Figure 2.10 shows the experimental loop's negative slope VCO voltage-to-frequency characteristics. Here the loop is operating at a given loop bandwidth and gain with no external noise present. The initial frequency is 1023.0 Hz. The loop acquires at 1019.0 Hz. The transmitter frequency is then increased in one hertz increments until synchronization is lost (1027.0 Hz). The spikes are caused by self-noise effects which are discussed in the next section.

4. Noise Effects

There are different types of noise which affect the operation of the loop: noise generated within the DLTL (self-noise) and noise which exists at the demodulator output (external-noise). In this experiment the loop's performance is evaluated while operating in the presence of both self-noise and external-noise.

Self-noise occurs at the output of the loop correlators whenever the input m-sequences are not perfectly matched. The amount of noise depends on the degree of synchronization. Generation of this noise is seen by viewing the correlator output voltage as shown in Figure 2.4. Assume that some mechanism (frequency drift, internal compensation, etc.) causes near perfect synchronization. Then the m-sequences become exactly aligned and the AVM output becomes DC and there is no self-noise. As the degree of synchronization varies the m-sequences become misaligned and the AVM output becomes AC which is self-noise.



f_c = 6.3 Hz, G = 140, n(t) = 0.0

FIGURE 2.10 EXPERIMENTAL VCO VOLTAGE-TO-FREQUENCY CHARACTERISTICS

Experimentation shows that self-noise manifests itself as a lowpass signal which acts to distort the loop error voltage. This distortion causes the received and local m-sequences to slide back and forth in relation to each other. At the punctual correlator this movement causes the output to become distorted and attenuated. As f_d increases, the degree of synchronization decreases and this self-noise effect increases until synchronization is eventually lost.

The addition of external-noise causes further distortion of the loop error voltage and of the punctual correlator output. As more noise is added, the probability the loop will lose lock increases. Eventually, the effects of external-noise will dominate the effects of self-noise.

These noise effects become even more pronounced as the frequency offset f_d increases. This increased noise effect results as follows. An increase in frequency offset causes an increase in phase offset and a corresponding decrease in the punctual correlator's output voltage, the level from which data is extracted. As this level is reduced, the noise is more likely to corrupt a decision. Thus, an increase in f_d causes the effects of noise to be more pronounced resulting in an increase in the probability of error P_e as explained next.

With zero frequency offset, the phase offset between $m_r(t)$ and $m_p(t)$ is also zero. Here, we are operating at point C on the loop error voltage curves of Figure 2.9. Zero

phase offset results in a maximum output voltage from the punctual correlator (Figure 2.4) from which data can be extracted (Figure 2.3). As f_d increases the phase offset increases and the loop error voltage operating point shifts from point C toward points B and B' (Figure 2.9). This phase offset causes a decrease in the punctual correlator output voltage (Figure 2.4) and a corresponding decrease in the voltage level from which data can be extracted (Figure 2.3).

For a given value of f_d, the addition of noise causes these punctual correlator output voltage levels to become randomly distributed about their mean values. When $f_d = 0$, this mean value is maximum ($+v_p$) and decreases with increasing values of f_d as shown in Figure 2.11. Because this experiment's receiver utilizes noncoherent detection in conjunction with a correlation post-detection processing scheme, the exact form of these probability density functions (pdf) is unknown. It is assumed here that they approximate Gaussian characteristics as Figure 2.11 depicts. Here we have two identical pdf's associated with a binary decision which differ only by their means. The minimum probability of error occurs at a threshold corresponding to the maximum likelihood decision rule. In this case the threshold is zero volts. As f_d increases the resulting decrease in mean values causes these pdf's to converge which increases the areas where they overlap the decision threshold. An increase in overlap area corresponds to an

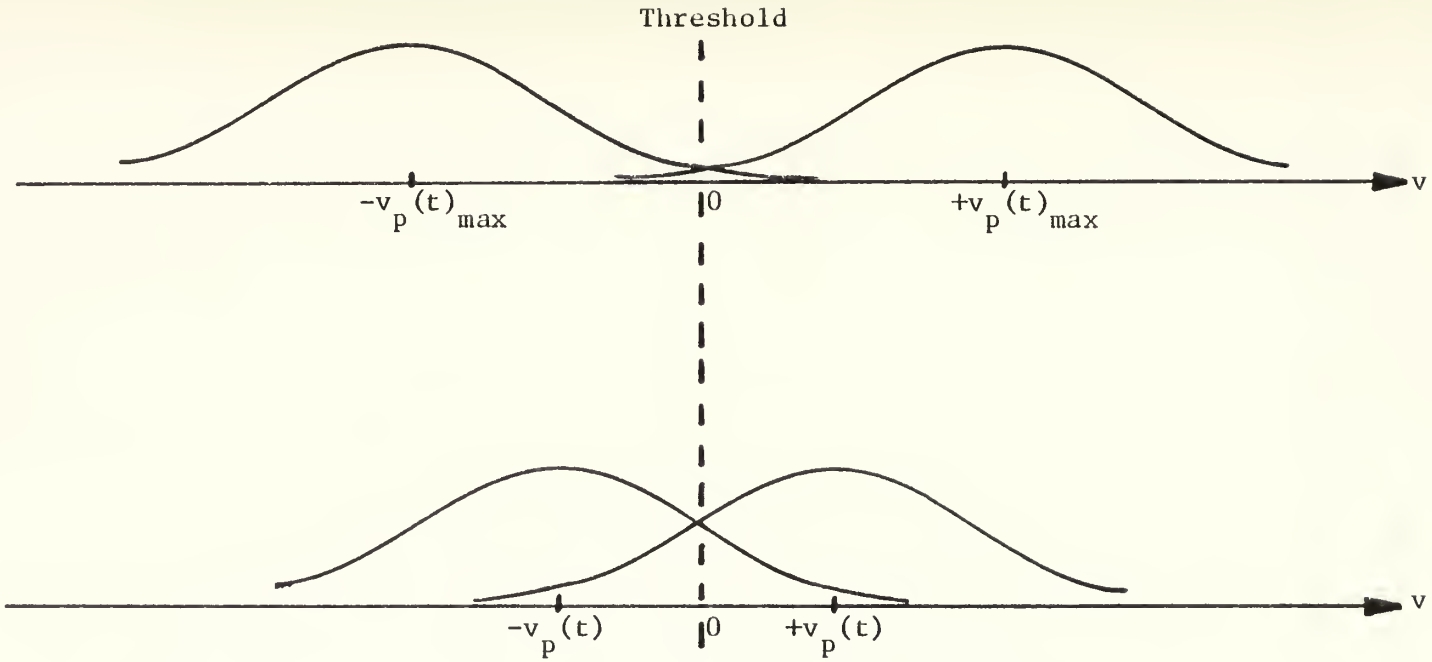


FIGURE 2.11 THEORETICAL PROBABILITY DISTRIBUTION FUNCTIONS FOR PUNCTUAL CORRELATOR OUTPUT VOLTAGES

increase in probability of error. Figure 2.12 shows pdfs which result from varying f_d for the experimental loop. Experimentation also shows that the loop captures at a maximum value of f_d while operating in the absence of noise. The difference frequency f_d must be decreased as the noise level increases for the loop to achieve a locked condition.

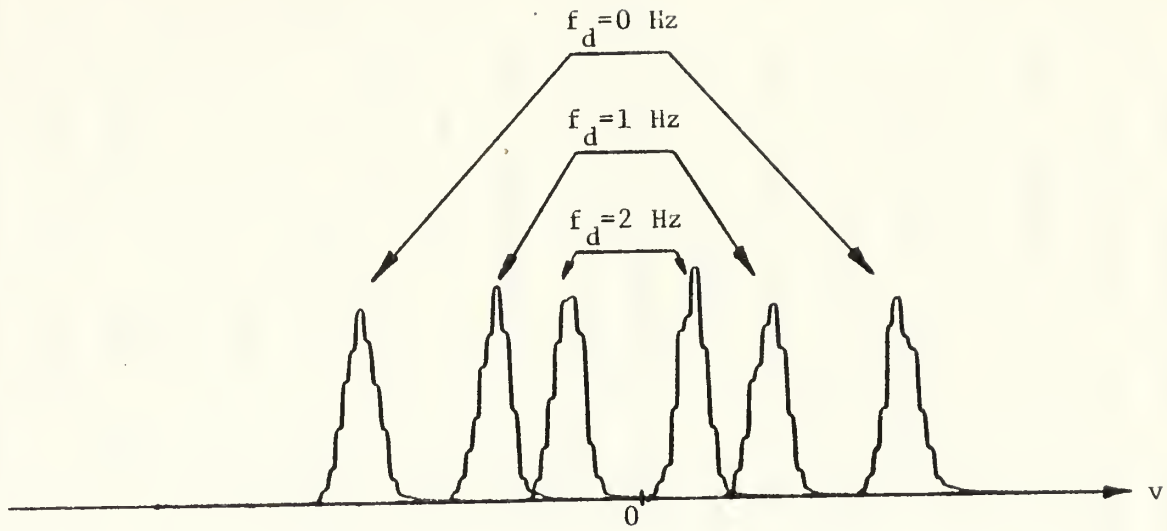


FIGURE 2.12 EXPERIMENTAL PROBABILITY DISTRIBUTION FUNCTIONS FOR PUNCTUAL CORRELATOR OUTPUT VOLTAGES

III. THE EXPERIMENTAL DELAY LOCK TRACKING LOOP

A block diagram of the experimental DLTL is shown in Figure 3.1. Again, the loop's process of synchronization is divided into three operational blocks: (1) m-sequence generation, (2) correlation, and (3) summation. In the first block, the loop employs a ten stage shift register (FSR) identical to the one found in the transmitter. Thus, by tapping the appropriate FSR stages, early and late and punctual replicas of the received m-sequence are generated. In block two, the early and late replicas are used by their respective loop correlators to generate voltage peaks whenever the received m-sequence correlates early or late. The data modifier circuitry that follows ensures that during correlation these voltage peaks always appear negative to the differential amplifier stage that follows regardless of the sequence received, $m_r(t)$ or its complement $\overline{m_r(t)}$. These voltage peaks are summed by a differential amplifier of block three in a early minus late gate fashion to form the initial version of the loop error voltage, $\hat{v}_d(t)$. This voltage is filtered by the loop filter and amplitude adjusted by the loop gain control. The combined effects of the loop filter's passband characteristics and the amount of loop gain determine the final form of the loop error voltage $v_d(t)$ and thus the loop's operating characteristics. To

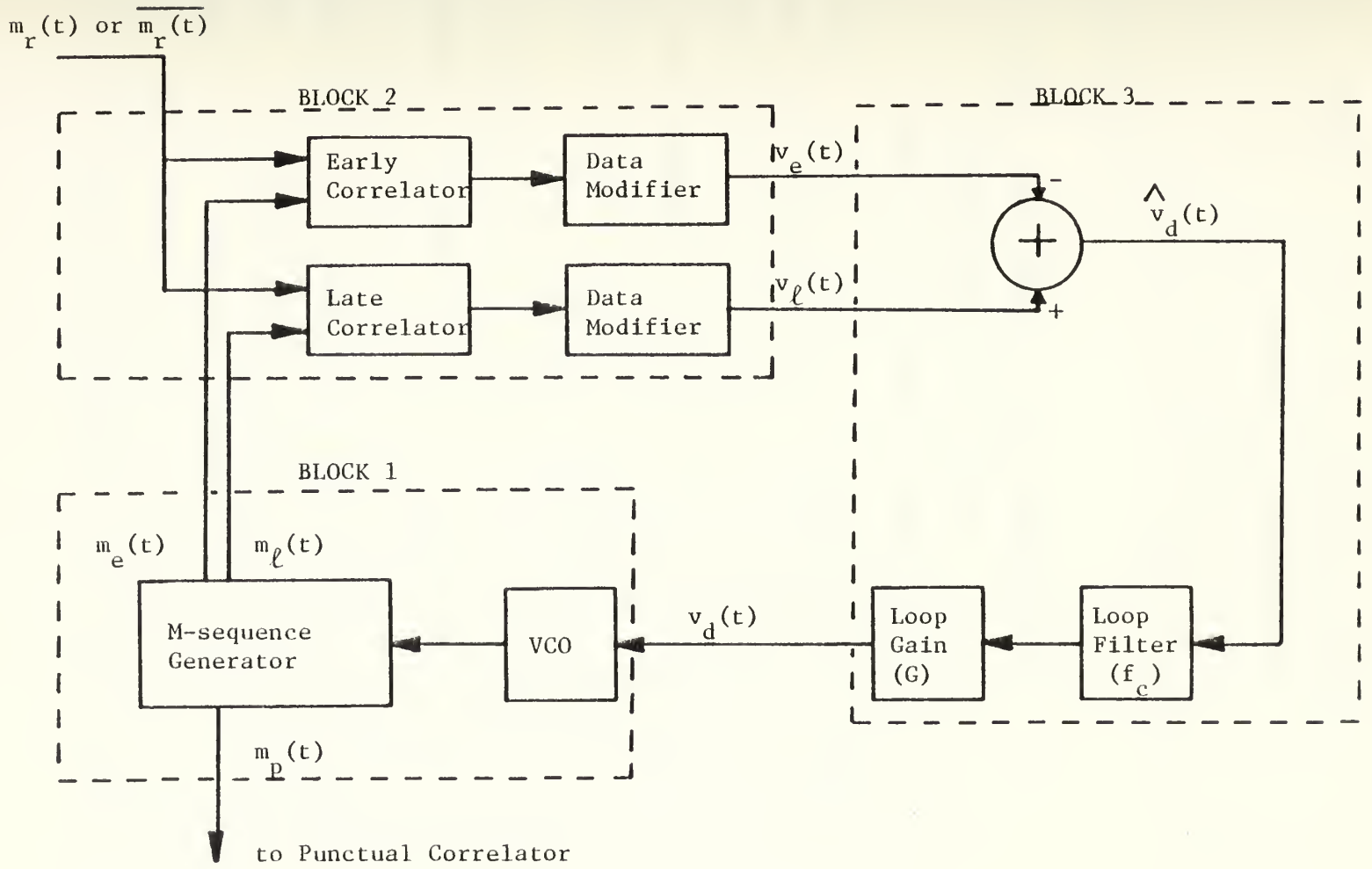


FIGURE 3.1 DELAY LOCK TRACKING LOOP BLOCK DIAGRAM

complete the loop, $v_d(t)$ is fed back to block one where it is used to drive the loop's VCO which clocks the local FSR and thereby changes the relative passing rate of the m-sequences. When synchronization occurs the punctual m-sequence is used by the punctual correlator to recover data. In the sections that follow the basic components of the loop are discussed.

A. DELAY LOCK TRACKING LOOP COMPONENTS

1. Feedback Shift Registers

Most direct sequence spread spectrum systems employ maximal length codes, or m-sequences, because of their desirable autocorrelation properties and their ease of generation. In this study a ten stage FSR is used to generate an m-sequence of length $2^{10}-1 = 1023$ chips. As described earlier, each m-sequence represents one data bit.

In this experiment the ten stage FSR is constructed by cascading two eight bit shift registers (74164). The outputs of stages three and ten are modulo-two summed with an EXNOR gate and fed back to the input stage as shown in Figure 3.2. This duplicates the transmitter's FSR configuration. All stages of the FSR are clocked synchronously. This results in a 1023 chip m-sequence appearing at the output of each stage. Each stage output is delayed in time by one chip from the stage that precedes it. To obtain early, punctual

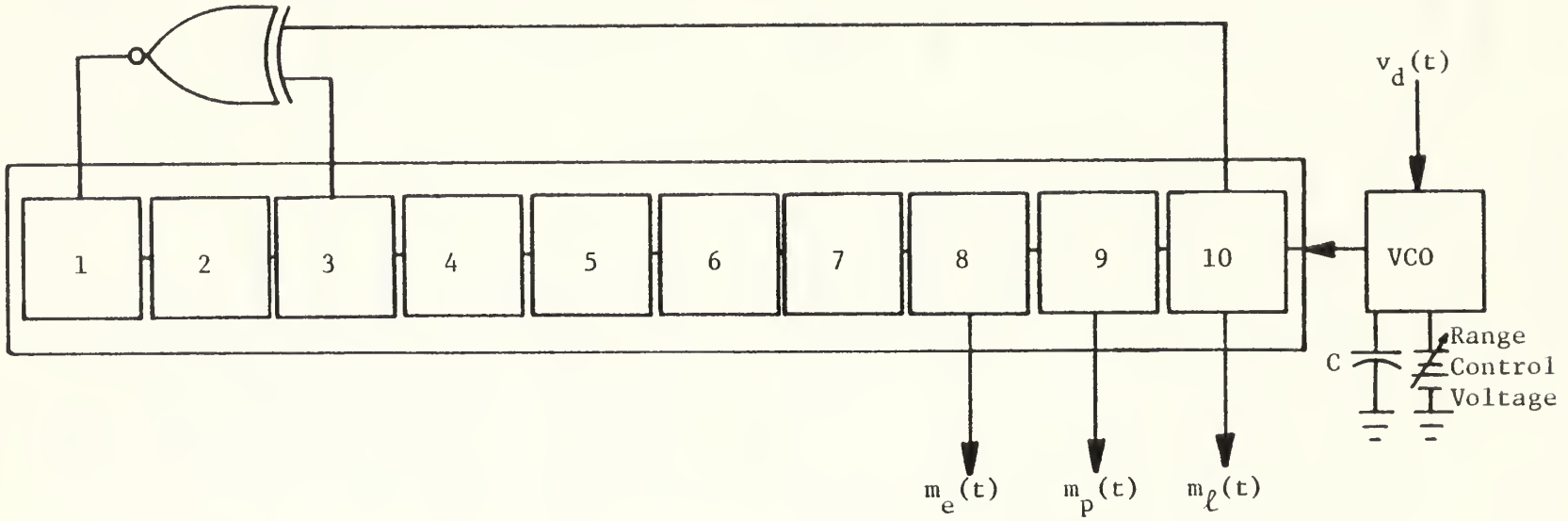


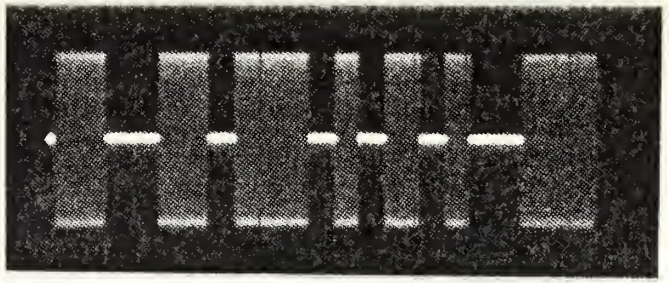
FIGURE 3.2 M-SEQUENCE GENERATOR

and late replicas of the received m-sequence, stages eight, nine, and ten are tapped respectively.

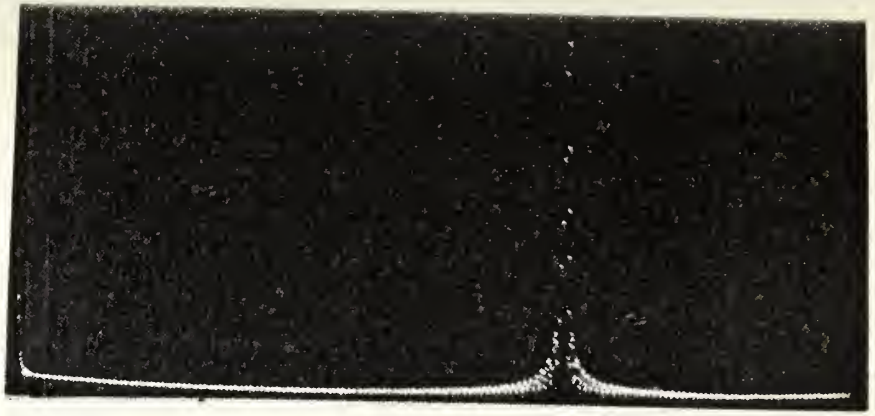
2. Loop Correlators

In this experiment, $m_r(t)$ results from the envelope detection of a 100 kHz sinusoidal carrier. Envelope detector inputs and outputs at various values of input SNR are shown in Figures 3.3 through 3.5. The time domain pictures show how the received signal becomes virtually lost in the noise as the SNR is decreased from -4 to -8 dB. The frequency domain pictures reveal the carrier, which is to be expected for on-off AM, but the data clock and the presence of data is masked by the noise. The data rate is one bit per second in this work. In the non-lock condition $m_r(t)$ is being received out of phase and frequency with its locally produced replica $m_p(t)$. Because of this frequency difference, these sequences will eventually pass each other causing the loop's early and late correlators to correlate first early then late or vice-versa. The correlation operation of block two is shown in Figure 3.6.

Correlation is achieved by first multiplying $m_r(t)$ with $m_e(t)$ or $m_\ell(t)$ and then averaging this product. Multiplication is accomplished by using $m_r(t)$ and the appropriate local replica as inputs to an analog voltage multiplier (AVM AD534) as shown in Figure 3.6. The variable DC voltages appearing at the differential inputs to the AVM perform a unipolar to bipolar conversion of the input signals. This



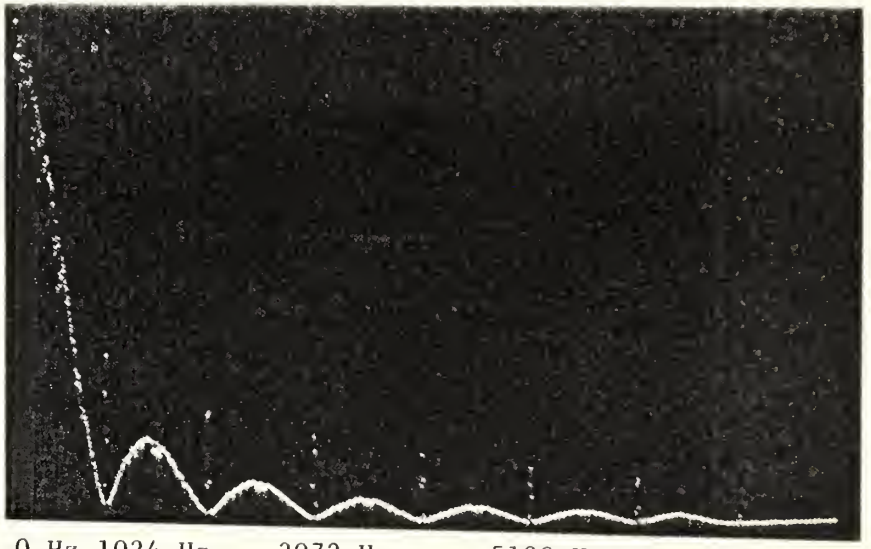
a) Input : Time Domain



0 kHz 100 kHz

b) Input : Frequency Domain, Bandwidth=2 kHz

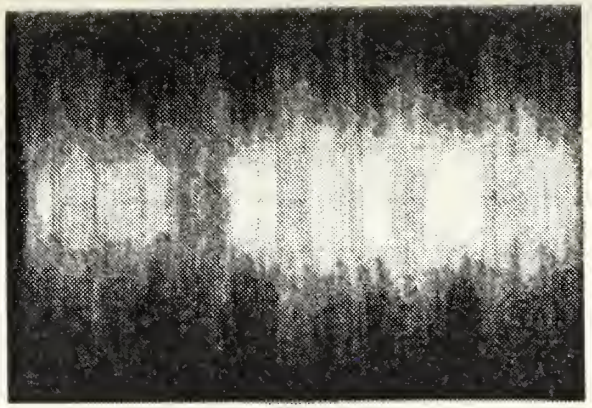
c) Output : Time Domain



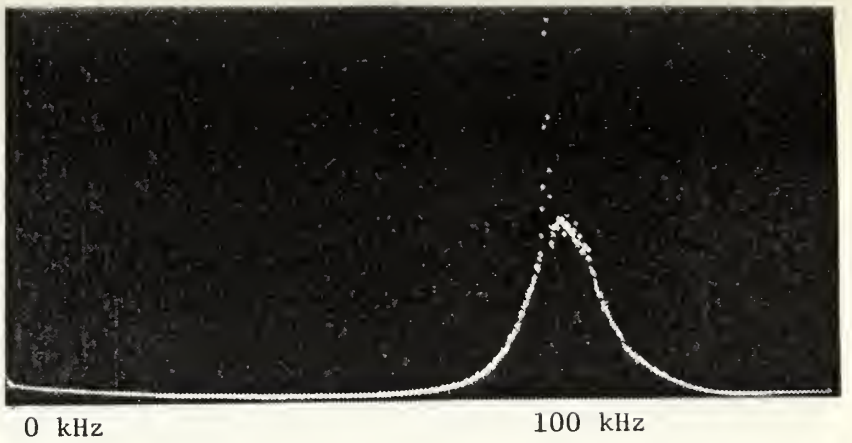
0 Hz 1024 Hz 3072 Hz 5120 Hz

d) Output : Frequency Domain

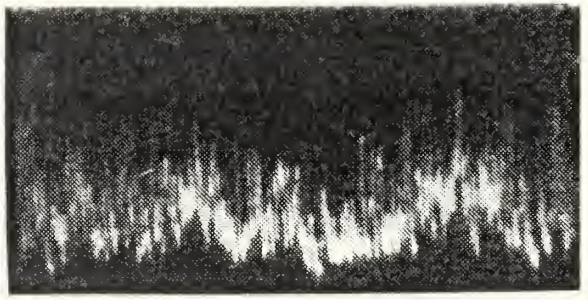
FIGURE 3.3 ENVELOPE DETECTOR INPUT (ASK) AND OUTPUT WHEN n(t)=0



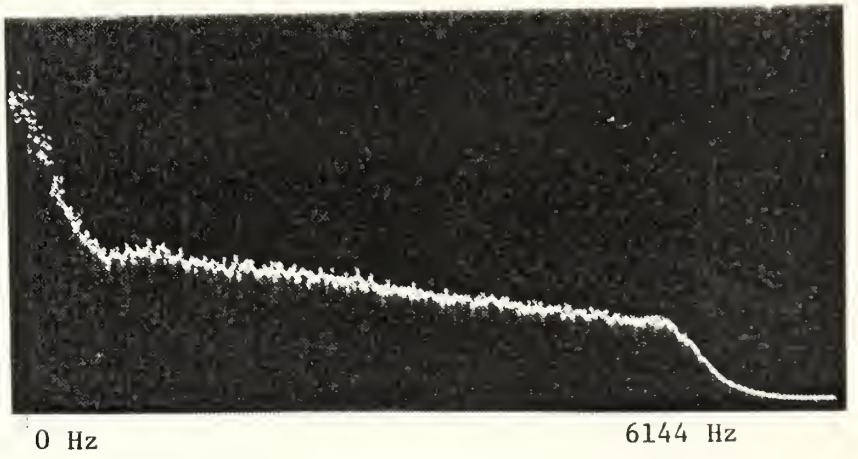
a) Input : Time Domain



b) Input : Frequency Domain, Bandwidth=2 kHz

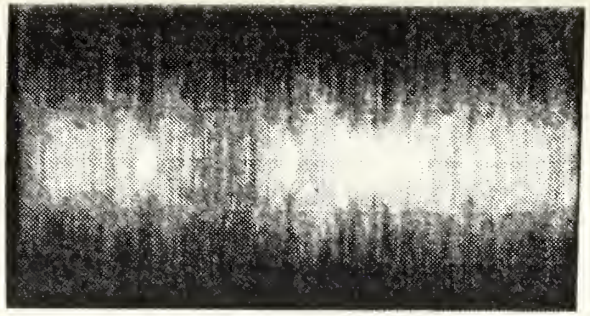


c) Output : Time Domain

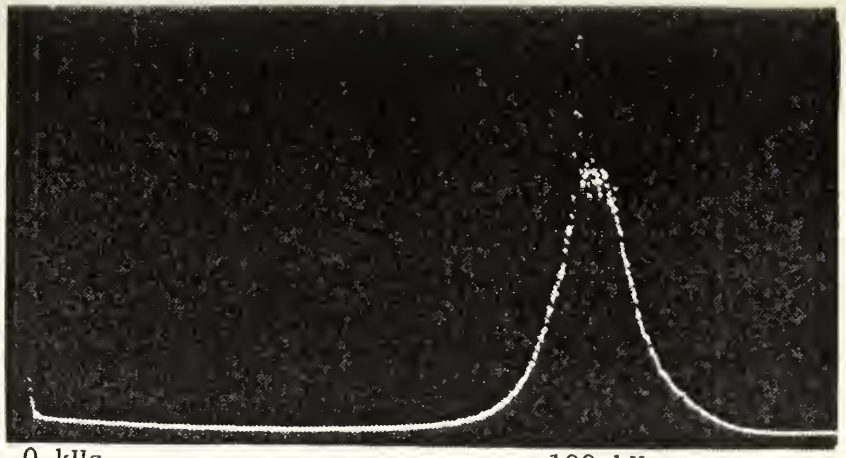


d) Output : Frequency Domain

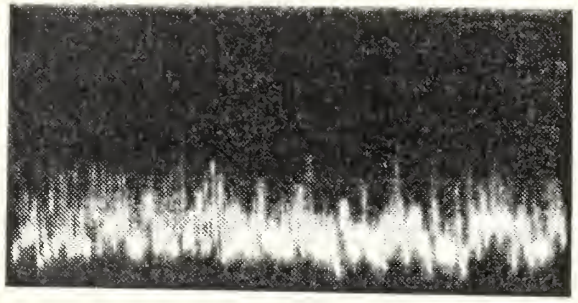
FIGURE 3.4 ENVELOPE DETECTOR INPUT (ASK) AND OUTPUT WHEN SNR = -4dB



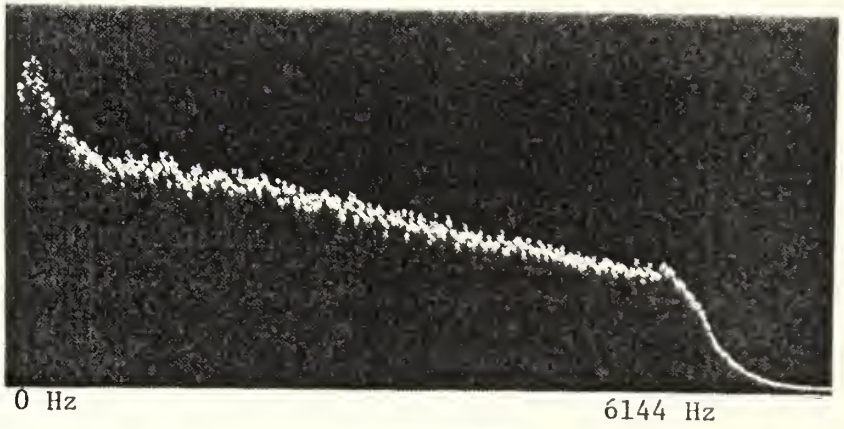
a) Input : Time Domain



b) Input : Frequency Domain, Bandwidth=2 kHz



c) Output : Time Domain



d) Output : Frequency Domain

FIGURE 3.5 ENVELOPE DETECTOR INPUT (ASK) AND OUTPUT WHEN SNR = -8dB

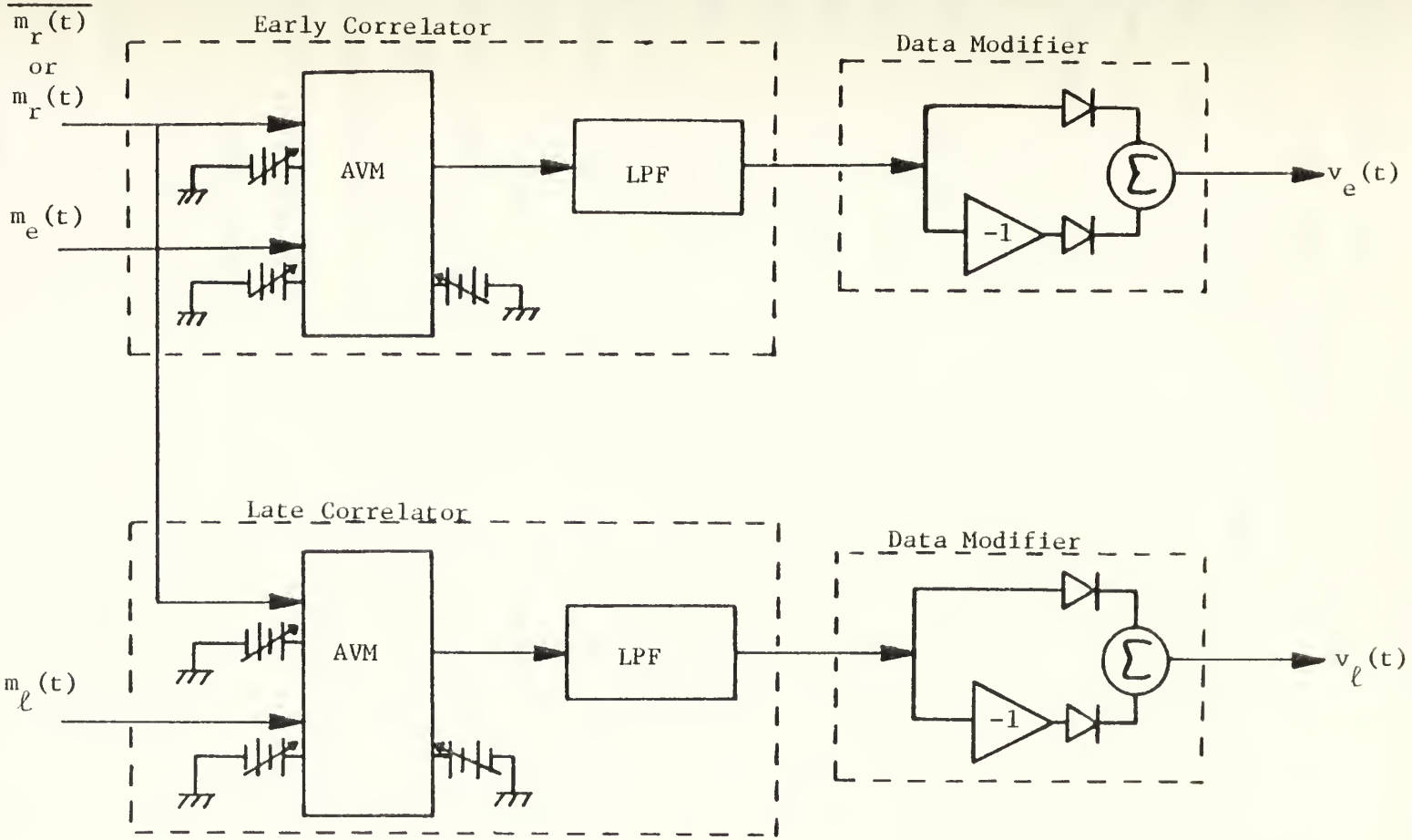


FIGURE 3.6 CORRELATOR CIRCUIT

conversion together with a variable DC output voltage adjustment ensures a positive or negative DC output whenever correlation occurs.

The AVM output is filtered by a fourth order Butterworth active filter (LM747) to complete the correlation operation. The filter performs the integration or averaging function of correlation. It has a design cutoff frequency of 30 Hz. This cutoff was determined experimentally to reduce the effects of data switching noise. In the initial design of the loop, correlator bandwidths were designed to match the desired loop capture rate. However, these relatively low bandwidths (2.3 to 6.3 Hz) prevented the correlator output voltage from adequately following the data transitions. This inadequate response caused voltage irregularities which eventually distorted the loop error voltage. The increased bandwidth of the correlator filter allows the correlator to respond more quickly which allows the data modifier circuitry to perform more effectively. As a result, the role of the correlator filter is to provide the appropriate correlation voltage and the role of the loop filter that follows is to establish the loop bandwidth.

3. Data Modifier

Because the received m-sequence has been modulated by data, either $m_r(t)$ or $\overline{m_r(t)}$ is received. As a result the outputs of the loop correlators can be either positive or negative correlation voltages. Because the experimental loop

operates on the basis of an early minus late gate error voltage, it is necessary that correlator output voltages appear consistently as either both negative voltages or as both positive voltages to the differential amplifier stage that follows. This is accomplished by data modifying (rectifying) the correlator output voltages.

Data modification is accomplished by the circuit shown in Figure 3.6. Operational amplifiers are used throughout to construct ideal doides, inverters, and summers.

The ideal diode circuit of Figure 3.7 eliminates the turn-on voltage of the diode which, if allowed to remain, would act to distort the loop error voltage. The ideal diode reduces this turn-on voltage (0.7 volts for silicon) to nearly zero volts by dividing this voltage by the forward gain of the operational amplifier.

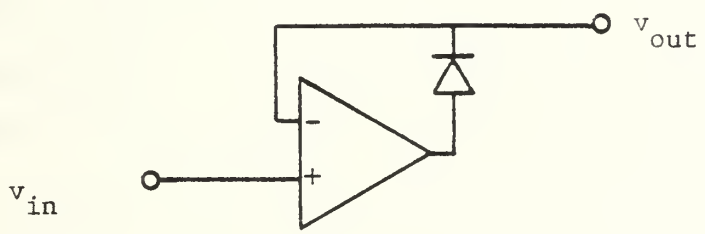


FIGURE 3.7 IDEAL DIODE CIRCUIT

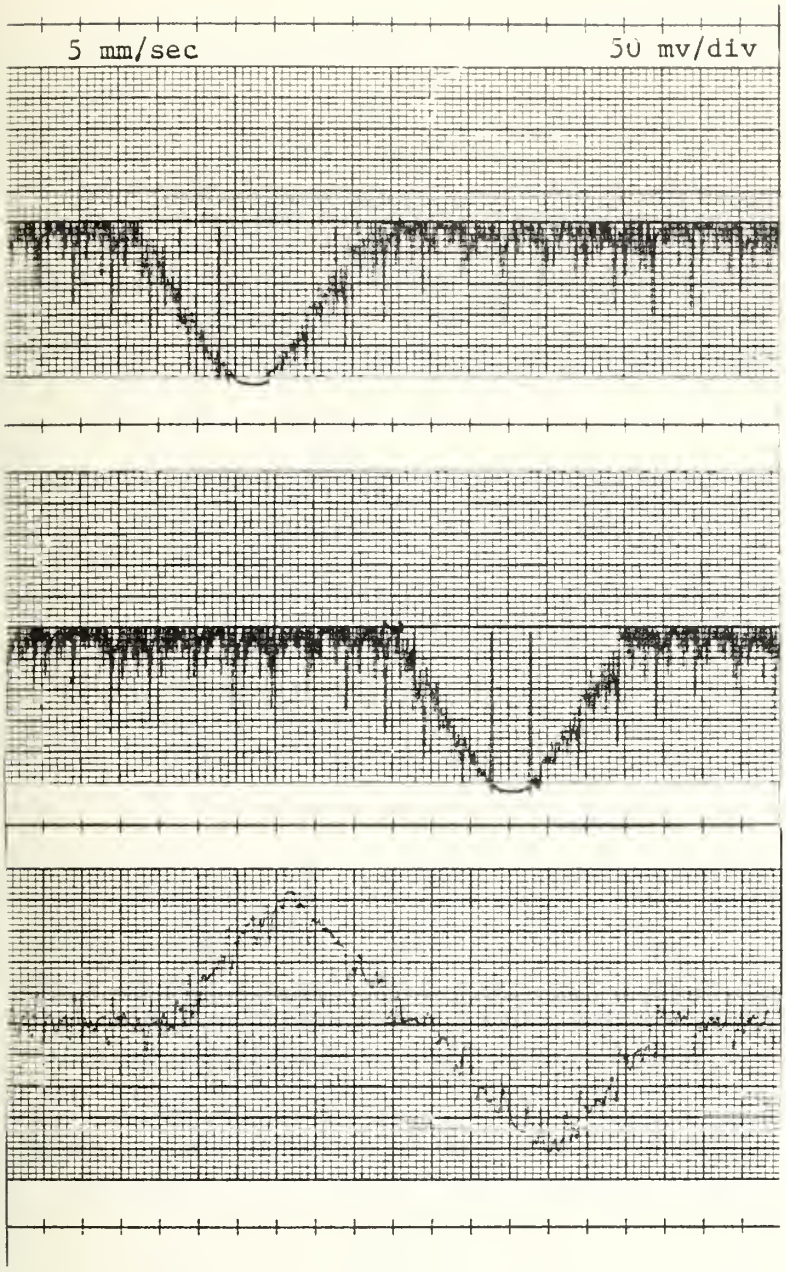
The data modifier circuit creates a negative absolute value function. The output of the modifier circuit is the negative value of whatever input voltage is applied. For example, a negative correlation voltage at the input is blocked by the upper branch diode and is inverted and then passed by the lower branch diode. This positive voltage is then inverted by the circuit's summing operational amplifier. Correlation voltages for the loop are shown in Figure 3.8. This voltage occurs for both "1" and "0" data bits.

4. Differential Amplifier

The differential amplifier (LM741) circuit shown in Figure 3.9 amplifies the difference of the early and late data modifier circuit outputs. This circuit generates the early minus late gate loop error voltage. In this experiment a late minus early voltage is used (Figure 3.8) because the data modifier circuitry provides negative correlation voltages and the VCO used has a negative slope VCO voltage-to-frequency characteristic.

5. Loop Filter

The loop filter in Figure 3.9 determines the bandwidth of the loop. The frequency response characteristics of this filter, in combination with the loop gain adjustment which follows, determine the acquisition and tracking characteristics of the loop. This filter is a fourth order Chebychev active filter (LM747) with a design cutoff



$v_e(t)$

$v_\ell(t)$

$v_d(t) = v_\ell(t) - v_e(t)$

f_c = 6.3 Hz, G = 140

$n(t) = 0$, f_d = 0.25 Hz

FIGURE 3.8 FORMATION OF LOOP ERROR VOLTAGE

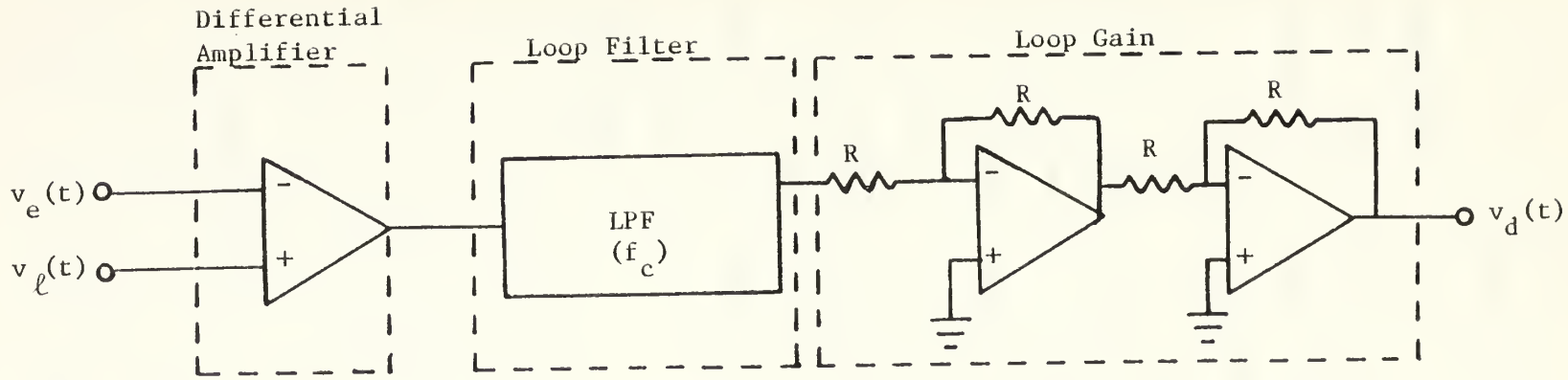


FIGURE 3.9 SUMMATION CIRCUIT

frequency f_c which is varied during this experiment (2.3, 4.0, 6.3 Hz). A Chebychev filter is chosen for its steep frequency cut-off characteristic.

6. Loop Gain

Loop gain control is accomplished by cascading two inverting operational amplifiers (LM747). Gain adjustments are made by adjusting two potentiometers, one at the input to each amplifier. For this experiment the range of adjustment for the relative gain G is from a point just short of where the gain causes the loop to become unstable to the point where further decreases in the gain cause no apparent effects in the loop's performance. The loop gain and bandwidth combination determine the operating characteristics of the loop by forming the final version of the loop error voltage which appears at the output of the summation circuit of Figure 3.9.

7. Loop Clock

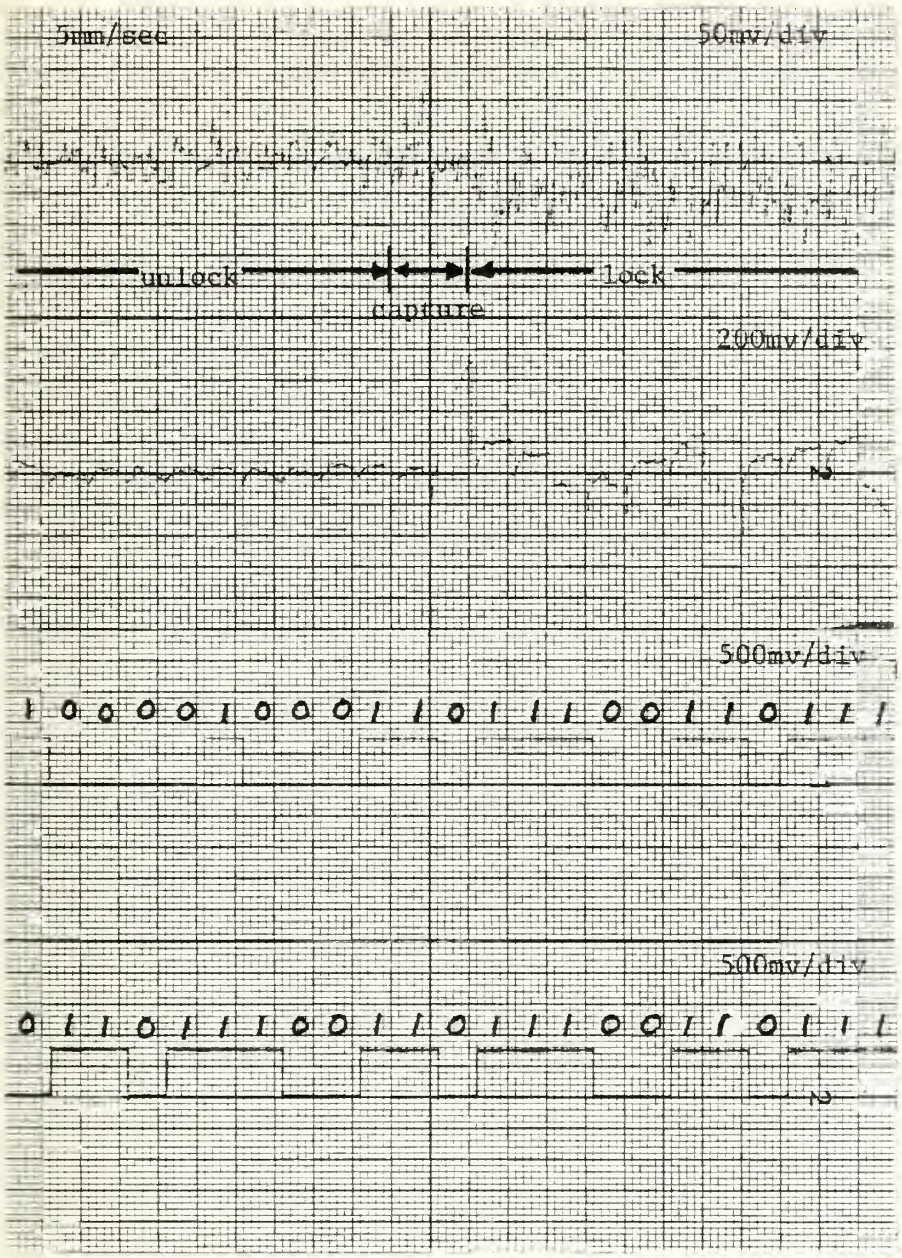
The loop clock appears as part of block one of Figure 3.2. Prior to synchronization, the loop clock determines the relative passing rate between the received m-sequence $m_r(t)$ and the locally generated replica $m_p(t)$. This clock is synchronized with the frequency of $m_r(t)$. The loop clock is constructed by using a voltage controlled oscillator (DM74124). The free running frequency of this VCO is determined by an external capacitor and a frequency range input voltage. The VCO's control voltage input is the loop

error voltage. In this way, the VCO output clock frequency changes in response to the loop error voltage.

B. DELAY LOCK TRACKING LOOP OPERATION

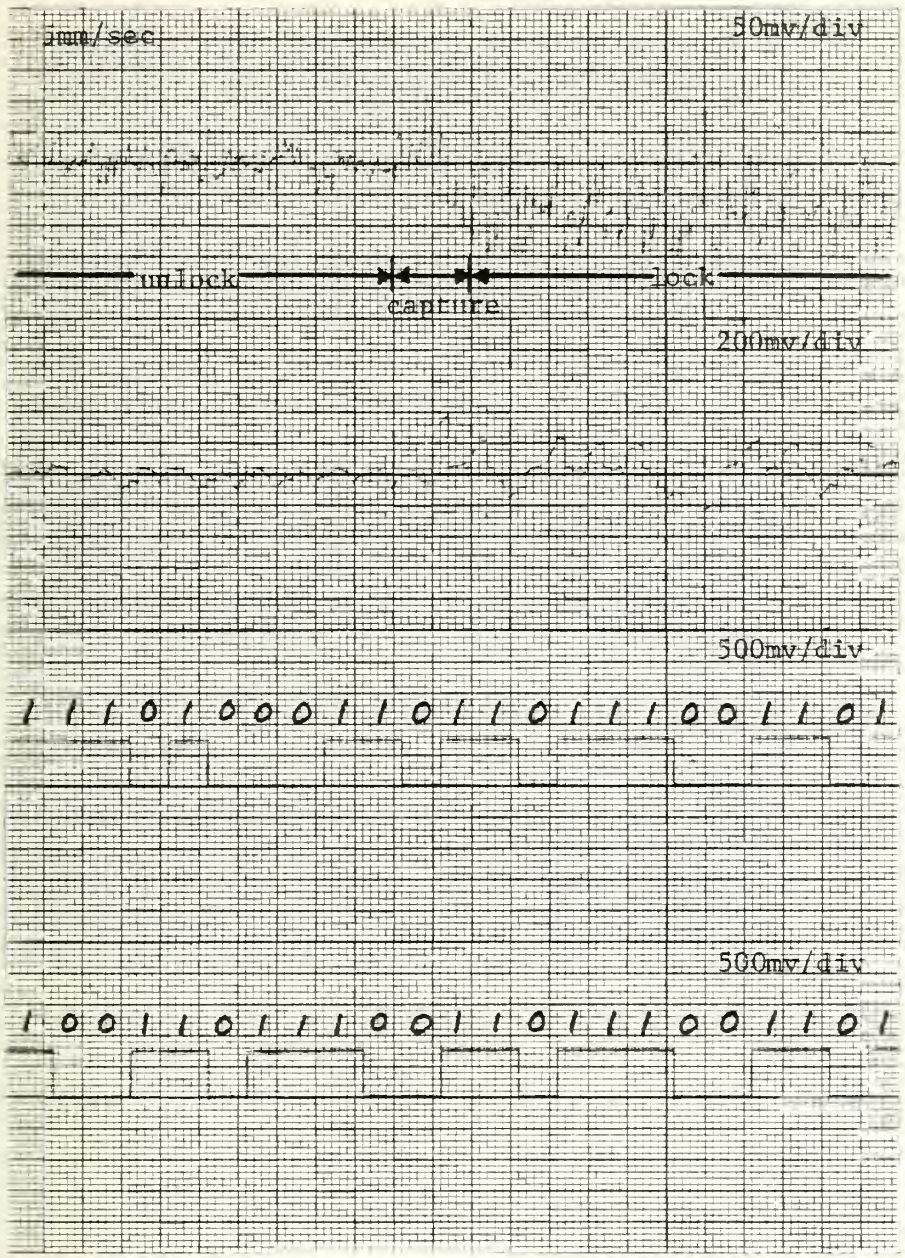
Loop error voltage traces and corresponding punctual correlator output, recovered data, and transmitted data are shown in Figures 3.10 through 3.18 for various combinations of loop parameters and operating conditions.

Figures 3.10 through 3.12 show the loop's capture characteristics. Figures 3.10 and 3.11 show the loop capturing at the lowest SNR for a given relative passing rate f_d. Note that a capturing process can be divided into three periods: unlock, transition, and lock. During the unlock period the loop error voltage $v_d(t)$ and the punctual correlator output $v_p(t)$ vary about zero volts. This causes the number of 1's and 0's recovered to be random. During the transition period the loop error voltage experiences a positive rise in voltage prior to stablizing. This initial positive voltage indicates that the loop experienced an early correlation followed by a late correlation. During the lock period $v_d(t)$ stablizes about a negative voltage level necessary to force the loop to follow the frequeny of the received m-sequence. During this period the received and punctual m-sequences are synchronized and data is recovered as shown. Figure 3.12 shows the effect of varying the loop



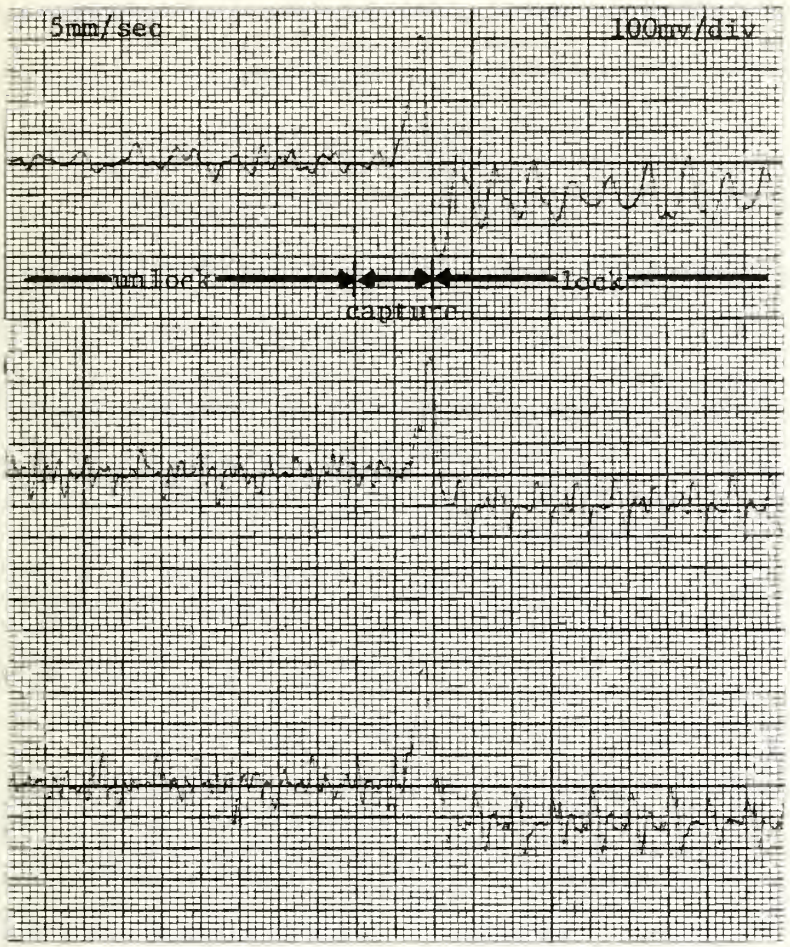
f_c = 6.3 Hz, G = 140

FIGURE 3.10 LOOP CAPTURE CHARACTERISTICS WHEN SNR = -7dB AND f_d = 1.0 Hz



f_c = 6.3 Hz, G = 140

FIGURE 3.11 LOOP CAPTURE CHARACTERISTICS WHEN SNR = -4dB and f_d = 2.0 Hz



f_c = 2.3 Hz

f_c = 4.0 Hz

f_c = 6.3 Hz

G = 140

f_d = 1.0 Hz, n(t) = 0

FIGURE 3.12 LOOP ERROR VOLTAGE VARIATIONS

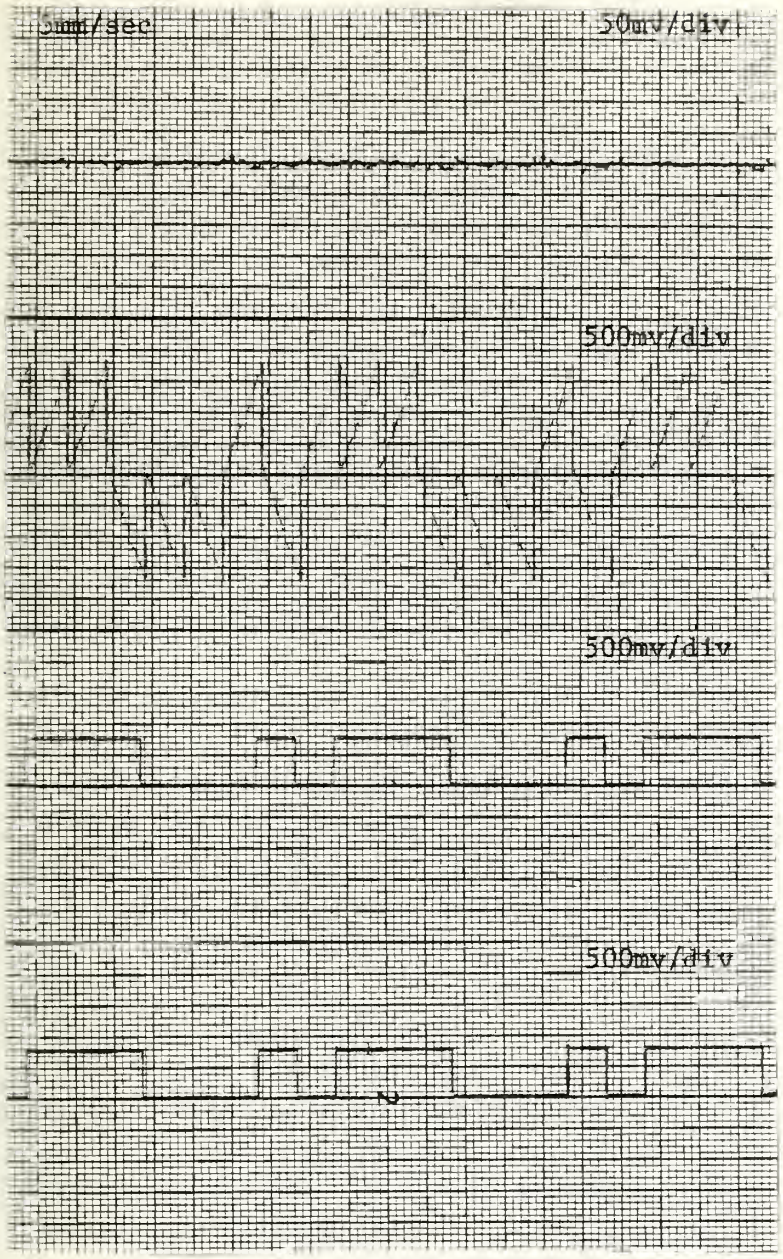
bandwidth on the loop error voltage. Note that as the loop bandwidth is increased from 2.3 Hz to 6.3 Hz, higher frequency components are passed by the loop and the loop error voltage variability increases.

Figures 3.13 through 3.18 show the loop's tracking characteristics. The effects of decreasing SNR for a zero Hz passing rate are shown in Figures 3.13 through 3.15. As the SNR decreases, $v_d(t)$ becomes contaminated with noise causing the received and local m-sequences to shift back and forth in relation to one another as they are correlating. This jittering causes the punctual correlator output to be attenuated and distorted.

For a fixed SNR of -4.0 dB, the effects of different passing rates are shown in Figures 3.16 through 3.18. As f_d increases, the effects of noise becomes more pronounced. The punctual correlator output becomes more attenuated and distorted as f_d increases as seen by comparing Figures 3.16 through 3.18.

C. EXPERIMENTAL PROCEDURES

During this experiment the loop's acquisition and tracking performance are evaluated under varying conditions of SNR and relative passing rate f_d. SNR and f_d are determined by following the systematic approach outlined below.



$v_d(t)$

$v_p(t)$

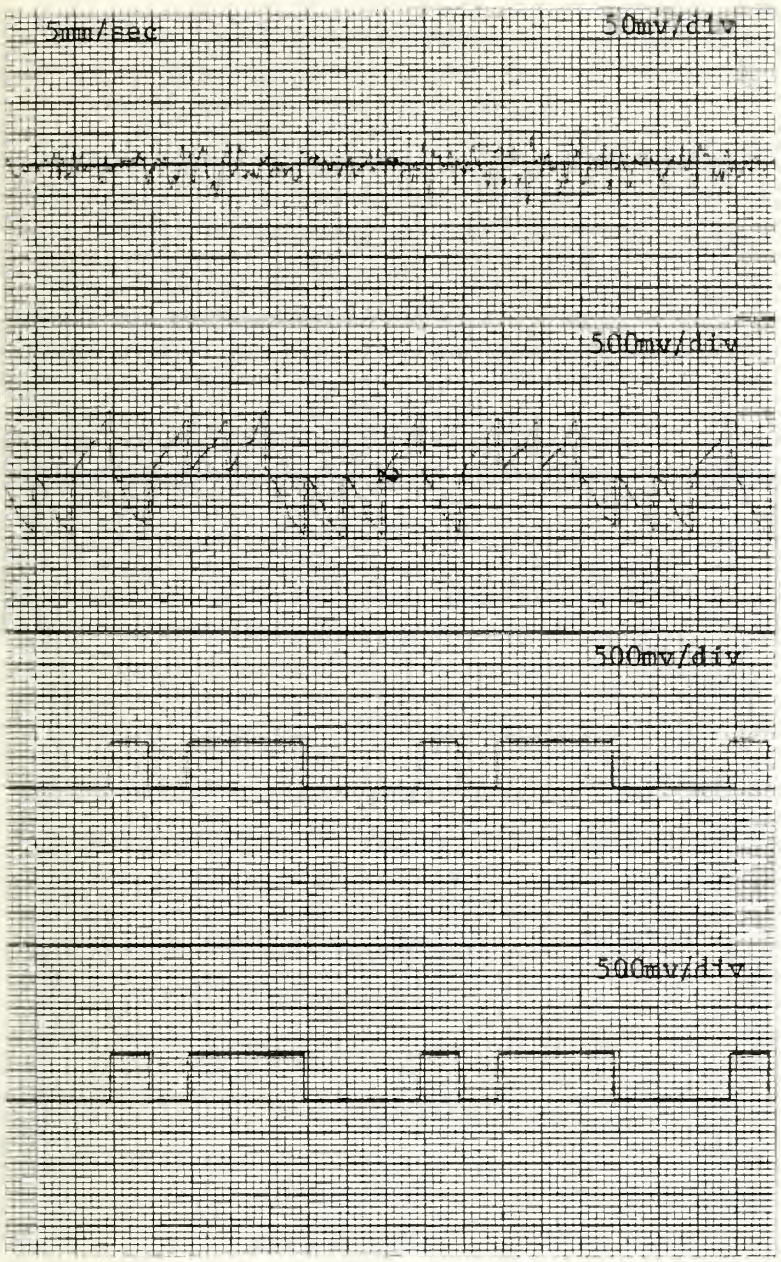
$\hat{d}(t)$

$d(t)$

f_c = 6.3 Hz, G = 140

f_d = 0.0 Hz, n(t) = 0

FIGURE 3.13 LOOP TRACKING CHARACTERISTICS
Scale of $v_p(t)$ is 500 mv/div.



$v_d(t)$

$v_p(t)$

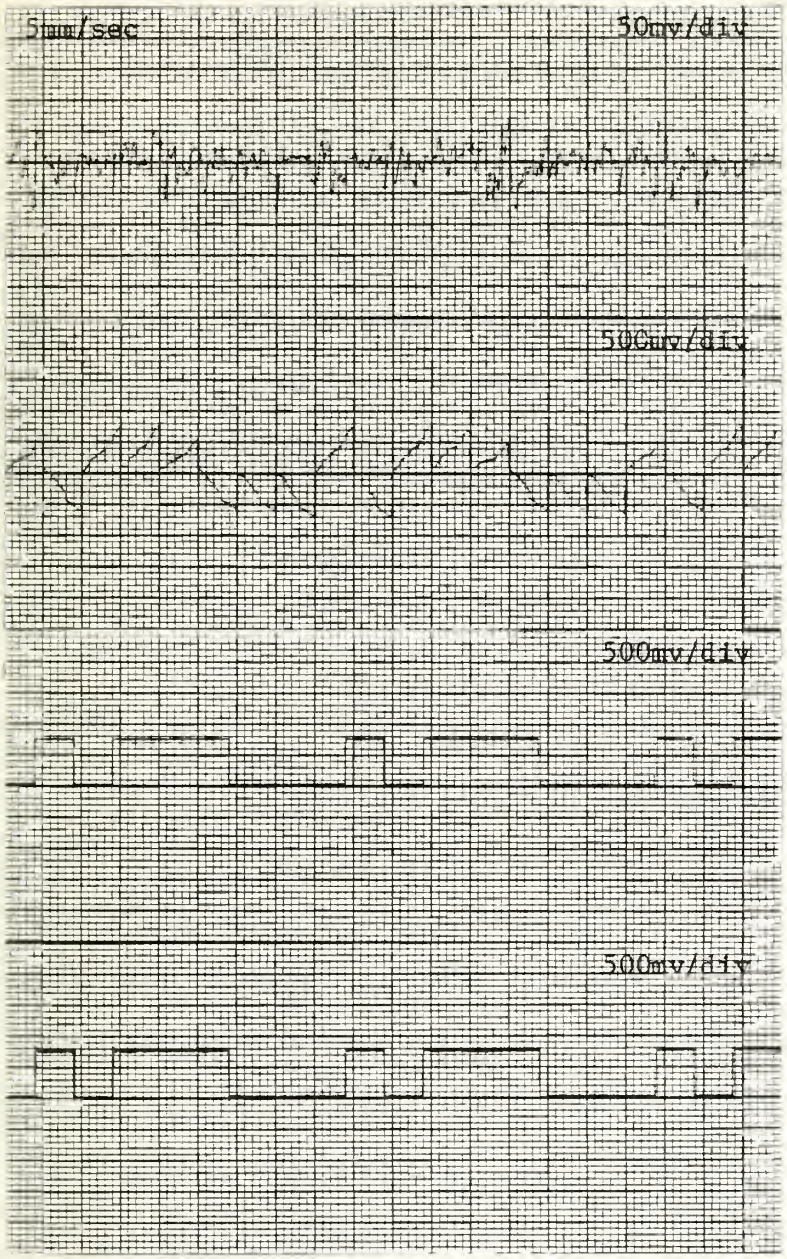
$\hat{d}(t)$

$d(t)$

f_c = 6.3 Hz, G = 140

f_d = 0.0 Hz, SNR = -4 dB

FIGURE 3.14 LOOP TRACKING CHARACTERISTICS
Scale of $v_p(t)$ is 500 mv/div.



$v_d(t)$

$v_p(t)$

$\hat{d}(t)$

$d(t)$

f_c = 6.3 Hz, G = 140

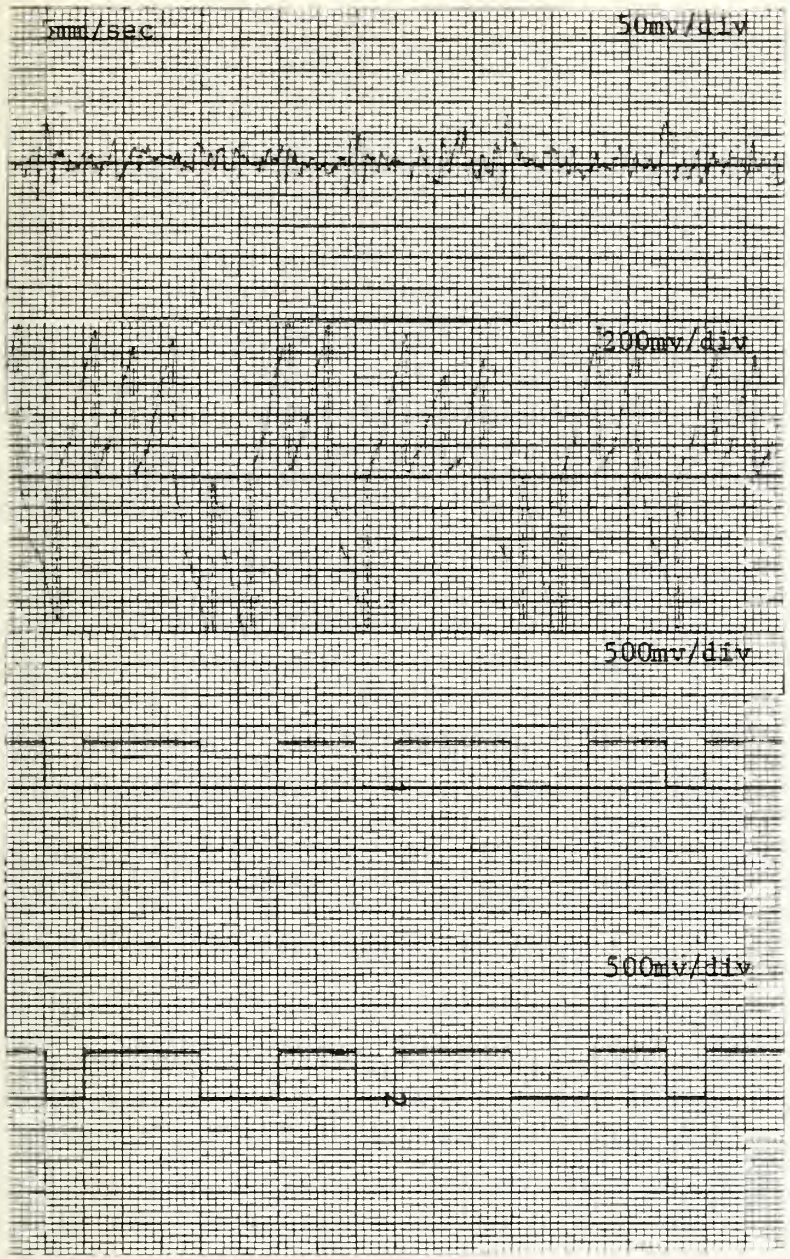
f_d = 0.0 Hz, SNR = -8 dB

FIGURE 3.15 LOOP TRACKING CHARACTERISTICS
Scale of $v_p(t)$ is 500 mv/div.

For this experiment, a constant signal voltage level of 0.3 volts RMS is maintained at the transmitter's AVM output (Figure 2.1). The normalized power associated with this signal is $(0.3)^2 = 0.09$ watts. Narrowband noise is added to the AVM's summing output to simulate the system's channel. The noise RMS voltage level is varied during the experiment to obtain the SNR of interest. At the demodulator input the SNR is determined by the following equation:

$$(SNR_{IN})dB = 10 \log\{ 0.09/[n(t)_{RMS}]^2 \} \qquad (2.1)$$

Before performance measurements are taken, the loop is placed in an initial operating state: the loop is tracking with an f_d of zero Hz. This initial condition is obtained by first forcing the system to lock and then by making loop fine adjustments. The locked condition is achieved by simultaneously resetting the m-sequence generators in both the transmitter and the receiver. Fine adjustments are conducted in two steps. In the first step, the early and late correlator outputs are made equally bipolar by adjusting the appropriate correlator AVM inputs as discussed earlier. The second step involves setting the transmitter frequency to some nominal value (1023.0 Hz) and then adjusting the VCO frequency range control voltage until the loop error voltage is minimum. At this point the loop error voltage is nearly zero volts and there is a minimum phase offset between $m_r(t)$ and $m_p(t)$.



$v_d(t)$

$v_p(t)$

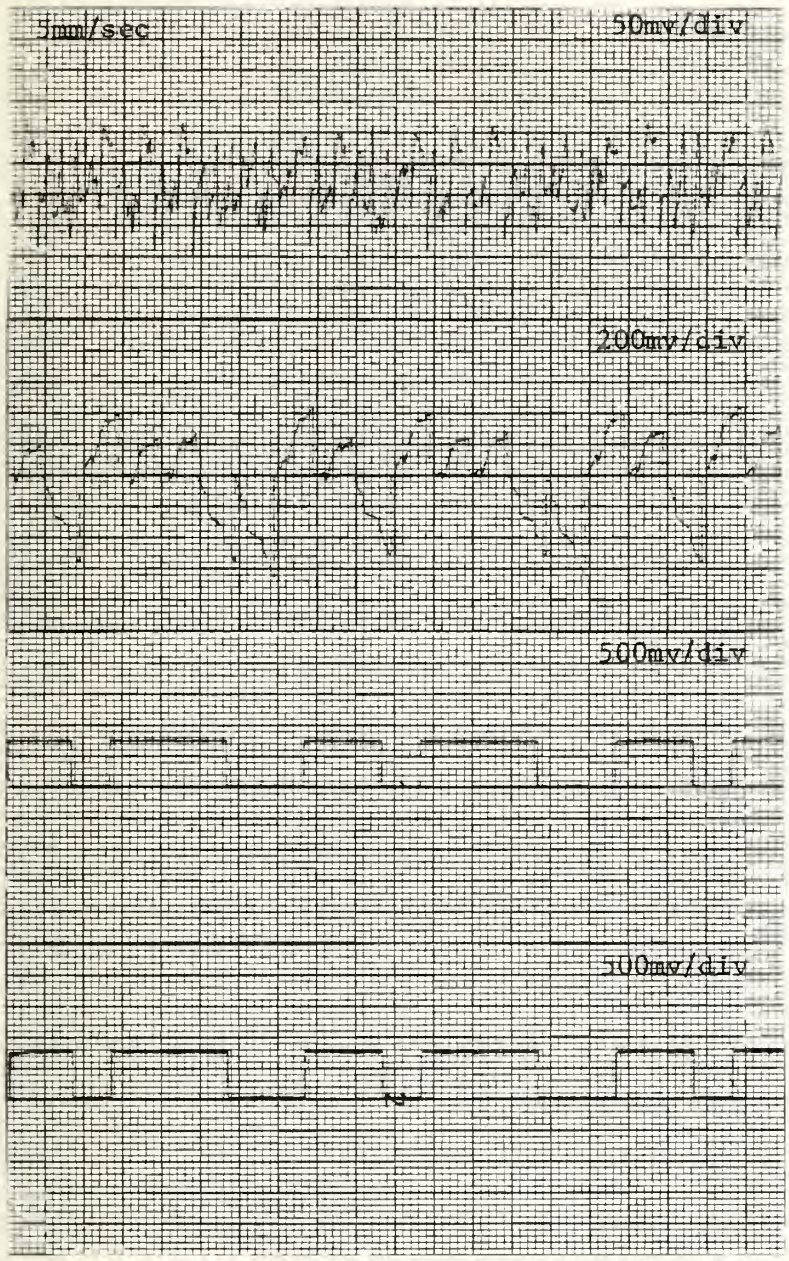
$\hat{d}(t)$

$d(t)$

f_c = 6.3 Hz, G = 140

f_d = 0.0 Hz, SNR = -4 dB

FIGURE 3.16 LOOP TRACKING CHARACTERISTICS
Scale of $v_p(t)$ is 200 mv/div.



$v_d(t)$

$v_p(t)$

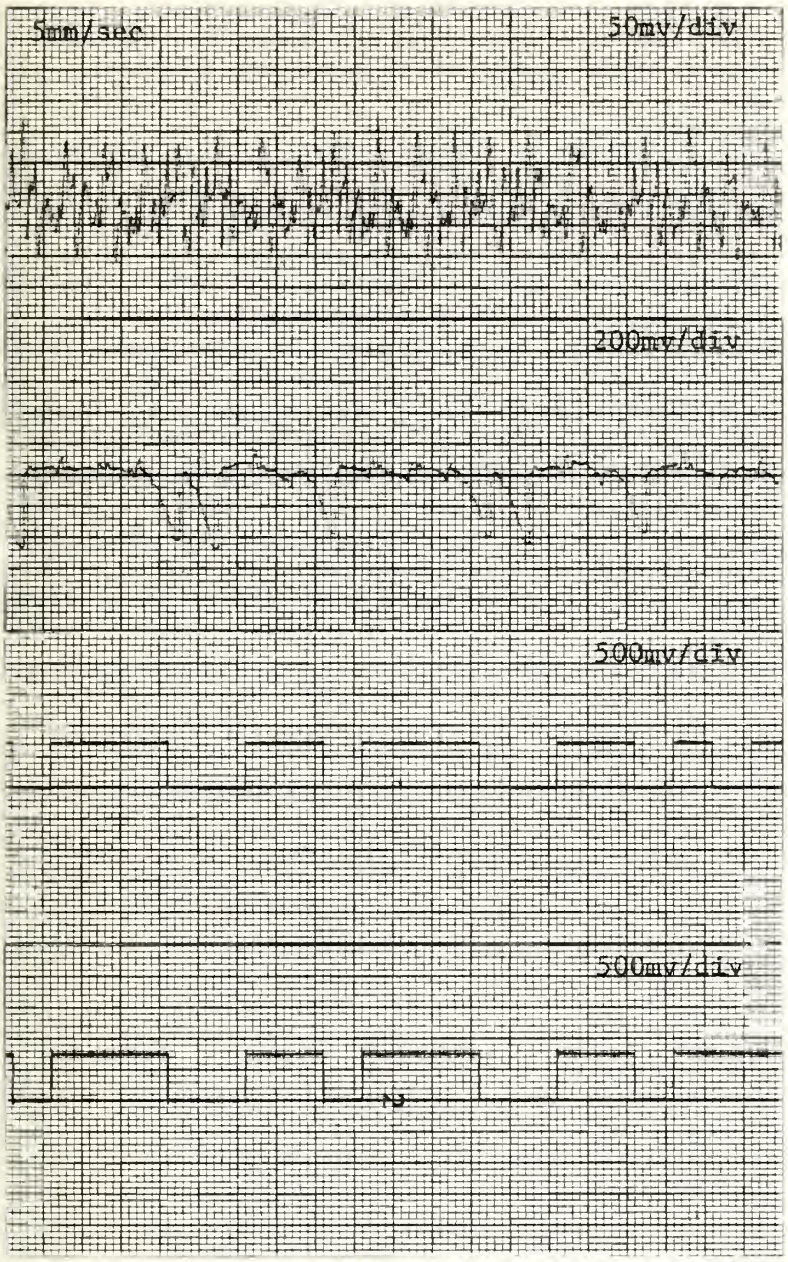
$\hat{d}(t)$

$d(t)$

f_c = 6.3 Hz, G = 140

f_d = 1.0 Hz, SNR = -4 dB

FIGURE 3.17 LOOP TRACKING CHARACTERISTICS
Scale of $v_p(t)$ is 200 mv/div.



$v_d(t)$

$v_p(t)$

$\hat{d}(t)$

$d(t)$

f_c = 6.3 Hz, G = 140

f_d = 2.0 Hz, SNR = -4 dB

FIGURE 3.18 LOOP TRACKING CHARACTERISTICS
Scale of $v_p(t)$ is 200 mv/div.

Once the initial operating condition is established, appropriate changes are made in SNR or f_d to evaluate the loop's tracking or capturing performance. Tracking evaluation is accomplished by simply adjusting the SNR for a given f_d. To evaluate the loop's capturing performance at a SNR of interest, the loop is forced out of the lock condition by increasing or decreasing the transmitter's frequency enough so that f_d is greater than the effective bandwidth of the loop. Once out of lock, the transmitter's frequency is reversed to the capture rate of interest. When capture occurs, the SNR is further decreased to determine the tracking performance after capture at the given value of f_d.

IV RESULTS AND CONCLUSIONS

A. RESULTS

A primary result of this study is that the direct sequence spread spectrum communications system considered in this experiment can operate noncoherently by means of a delay lock tracking loop at SNRs as small as -5.0 to -7.1 dB. Tables I through III show these results for various loop parameter settings and operating conditions.

The two loop parameters studied in this experiment are loop gain and bandwidth. Although an increase in either parameter allows the loop to acquire at lower SNR and/or at greater relative passing rates, the effects of changes in loop gain seem to dominate the effects of changes in loop bandwidth. For example, at a loop bandwidth setting of 6.3 Hz, an increase in relative gain from 60 to 140 allows a -2.3 dB change in SNR for capture at an f_d of 1.0 Hz, whereas a loop bandwidth increase from 2.3 to 6.3 Hz allows only a -0.8 dB change in SNR for the same capture rate. The primary effect of loop bandwidth increase is to allow the gain setting to be varied over a greater range of values. As such, combined changes in loop bandwidth and gain have the greatest effect on the loop's performance. For example, a change of loop bandwidth from 2.3 to 6.3 Hz in conjunction

with a loop gain change from 40 to 140 allows a 5.8 dB reduction in SNR to lose lock for an f_d of 1.0 Hz.

TABLE I

LOCK AND CAPTURE CHARACTERISTICS

Loop bandwidth = 2.3 Hz

f_d	0.0 Hz	1.0 Hz		2.0 Hz	
GAIN	AVG SNR TO LOSE LOCK (dB)	AVG SNR TO CAPTURE (dB)	AVG SNR TO LOSE LOCK AFTER CAPTURE (dB)	AVG SNR TO CAPTURE (dB)	AVG SNR TO LOSE LOCK AFTER CAPTURE (dB)
80	-11.2	-5.0	-5.3	-1.0	-1.9
60	-10.7	-3.9	-4.9	-	-
40	-10.6	-1.3	-1.7	-	-
20	-8.9	-	-	-	-

TABLE II

LOCK AND CAPTURE CHARACTERISTICS

Loop Bandwidth = 4.0 Hz

f_d	0.0 Hz	1.0 Hz		2.0 Hz	
GAIN	AVG SNR TO LOSE LOCK LOCK (dB)	AVG SNR TO CAPTURE CAPTURE (dB)	AVG SNR TO LOSE LOCK LOCK AFTER CAPTURE (dB)	AVG SNR TO CAPTURE CAPTURE (dB)	AVG SNR TO LOSE LOCK LOCK AFTER CAPTURE (dB)
150	-10.3	-6.2	-7.2	-3.5	-4.7
130	-10.7	-5.8	-6.3	-3.5	-4.7
100	-10.4	-5.5	-6.4	-3.3	-4.5
80	-9.6	-5.0	-5.5	-1.6	-2.8
60	-8.9	-4.2	-4.7	+2.18	+0.2

TABLE III

LOCK AND CAPTURE CHARACTERISTICS

Loop Bandwidth = 6.3 Hz

f_d	0.0 Hz	1.0 Hz		2.0 Hz	
GAIN	AVG SNR TO LOSE LOCK LOCK (dB)	AVG SNR TO CAPTURE CAPTURE (dB)	AVG SNR TO LOSE LOCK LOCK AFTER CAPTURE (dB)	AVG SNR TO CAPTURE CAPTURE (dB)	AVG SNR TO LOSE LOCK LOCK AFTER CAPTURE (dB)
140	-10.4	-7.1	-7.9	-4.0	-5.2
120	-9.5	-7.1	-7.8	-4.0	-5.2
100	-9.4	-6.9	-7.6	-2.5	-3.1
80	-10.1	-5.8	-6.3	-1.3	-1.5
60	-10.4	-4.8	-5.3	+0.62	-1.4

Another significant result of this study is the design and successful use of a circuit which modifies data so that the loop can acquire and track m-sequences modulated by the data. This circuit is shown in Figure 3.6 and its operation is explained in Section III.A.3.

Also, this study shows in theory and in experimentation how operating at a certain frequency offset f_d allows the effect of noise to be more pronounced. The theory is discussed in Section II.C.4. The experimentation conducted in this study supports this theoretical result. As shown in Tables I through III, an average of 3.0 dB improvement in SNR is required to capture at twice the passing rate for a given loop bandwidth and gain setting.

B. CONCLUSIONS

Completely asynchronous (noncoherent) detection of AM signals is possible at negative decibel signal-to-noise ratios. The delay lock tracking loop developed in this study appears suitable as a means for deriving a local code reference. Furthermore, the loop derives this local code reference whether or not the spreading signal is modulated by data.

A given loop bandwidth and gain setting establish the performance boundaries of the loop, i.e. how great the relative passing rate or how small the SNR can be for the loop to acquire lock. For a given application, tradeoffs can

be made between f_d and SNR. The larger the value of f_d, the larger the value of SNR needed to acquire and maintain lock, and vice-versa.

Various methods can be used to improve the performance of the loop. Two basic methods are (1) changing the form of the loop error voltage, and (2) making the loop filter adaptive. The first method involves the loop using two m-sequences which are displaced in time from each other by one chip interval instead of two chip intervals. Gill [Ref. 3] shows that this method realizes a 3 dB improvement in noise performance but can tolerate only half the relative passing rate. The second method involves using various search-lock strategies which allows the loop to lock at a much greater relative passing rates [Ref. 4].

APPENDIX A

LOOP BANDWIDTH-PASSING RATE RELATIONSHIP

Correlation occurs as two identical m-sequences $m_1(t)$ and $m_2(t)$, clocked at rates f_1 and f_2 Hz, slide past each other at some relative passing rate $f_d = f_2 - f_1$. As this correlation occurs, the DC portion of the correlator output will actually trace the autocorrelation function (ACF) of the m-sequence shown in Figure A.1. In this figure, L is proportional to the m-sequence length ($L=2^n-1$, where n is the number of FSR stages being used to generate the m-sequence). L indicates the relative magnitudes of the ACF peak and sidelobe levels.

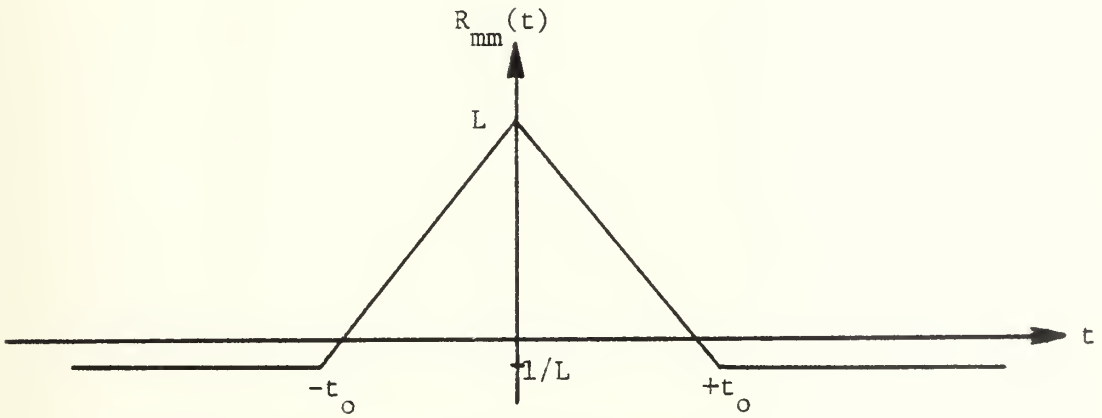


FIGURE A.1 M-SEQUENCE AUTOCORRELATION FUNCTION

At time t=0, $m_1(t)$ and $m_2(t)$ are in phase and the peak ACF voltage results. At time $t=t_o$, $m_1(t)$ and $m_2(t)$ are separated by one chip (one clock pulse) and the lowest sidelobe level is reached. Since $m_1(t)$ and $m_2(t)$ have a relative passing rate of f_d chips per second , then $t_o=1/f_d$.

The Fourier Transform of $R_{mm}(t)$ is the power spectrum of the m-sequence which has a $(\sin x / x)^2$ form with a commonly defined bandwidth $b_r = 1/t_o = f_d$. Therefore, the required loop bandwidth equals the sequence passing rate.

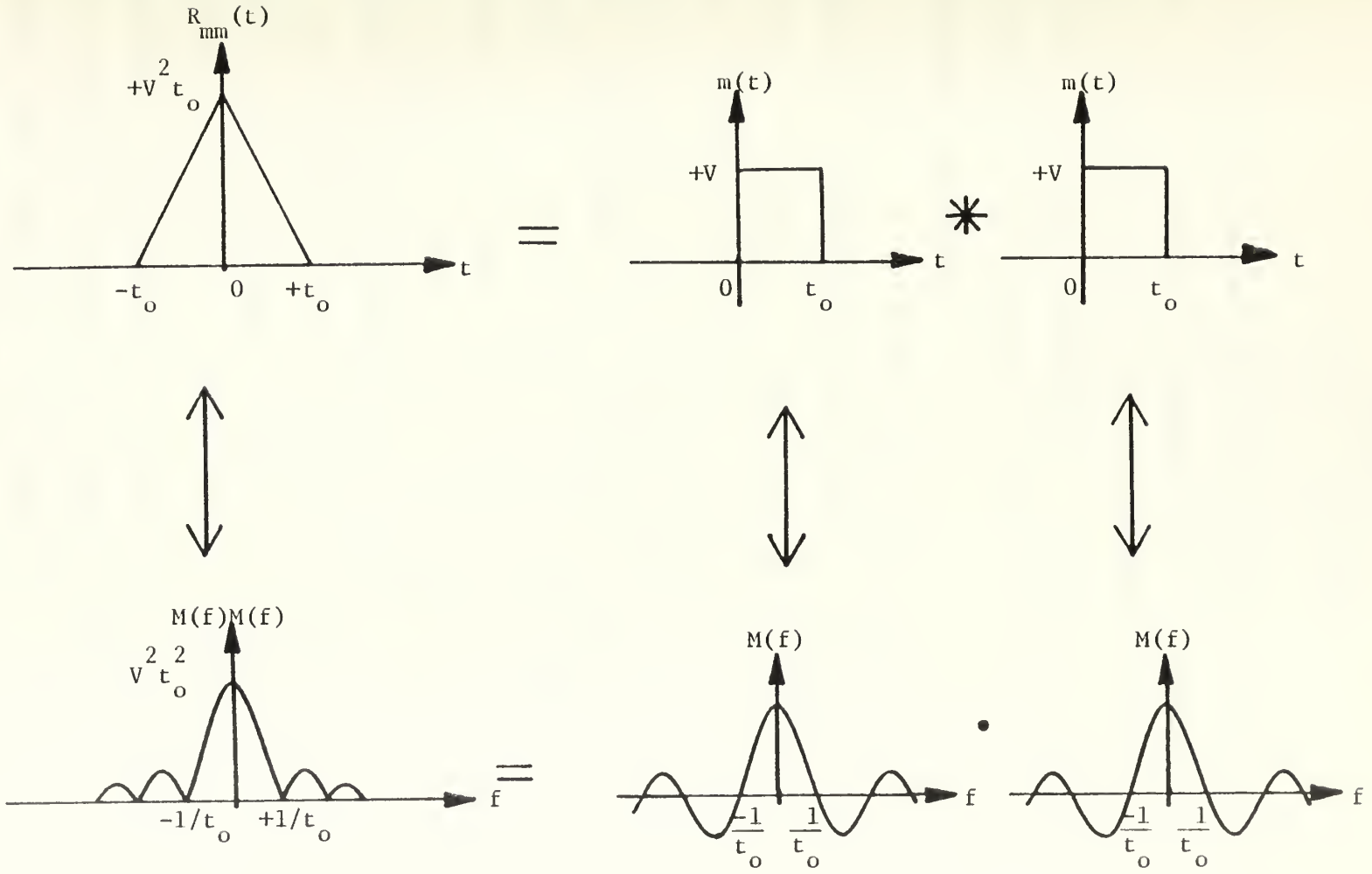


FIGURE A.2 CORRELATION BANDWIDTHS

APPENDIX B

CIRCUIT SCHEMATICS

This appendix contains the schematic diagrams for all of the circuits used in the experimental delay lock tracking loop. Standard digital and analog (MSI and LSI) monolithic chips are used throughout. Capacitor values are in microfarads and resistor values are in kilohms unless otherwise indicated.

Figure B.1 shows the loop clock and m-sequence generator with protection circuit. The loop clock's free running frequency is set by selecting an appropriate external capacitor value and adjusting two frequency control input voltages. One frequency control input is used to make fine adjustments of the clock's free running frequency (1023.0 Hz). The other control input uses the loop error voltage as its input. This causes the clock's output to vary in response to the loop. This clock output is applied directly to the m-sequence generator.

Two eight bit shift registers (74164) are cascaded to obtain the ten stages necessary to generate the local m-sequence replicas. To duplicate the transmitter's m-sequence generator, the outputs of the third and tenth stages are fed back through an EX-NOR gate (74266) whose output is serially loaded into the first shift register. Synchronous clocking of the registers together with the serial feedback generates

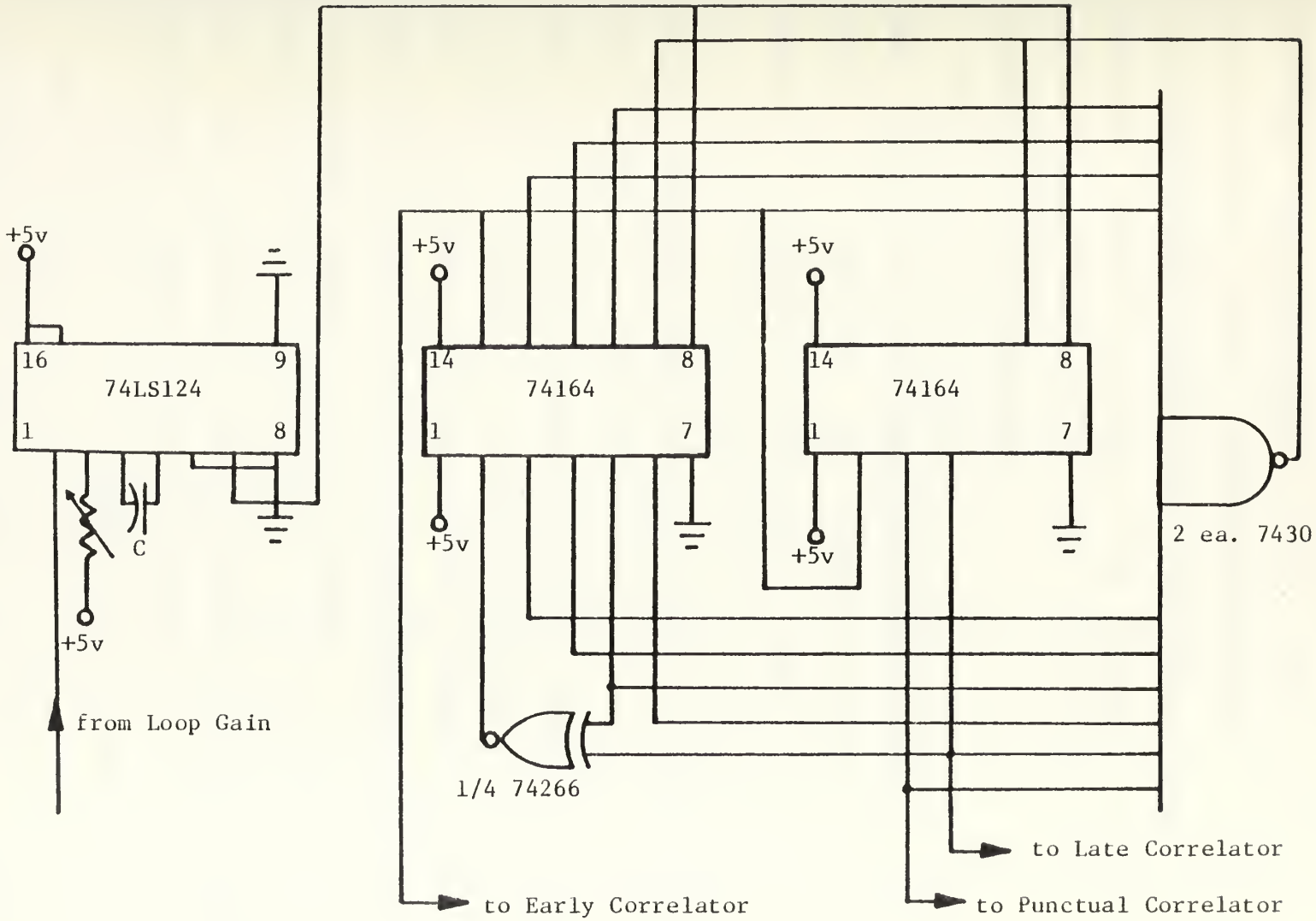


FIGURE B.1 LOOP CLOCK AND M-SEQUENCE GENERATOR WITH PROTECTION CIRCUIT

a 1023 chip m-sequence at the output of each stage. Thus, each succeeding stage output is delayed in time by one chip interval from the preceding stage. Early, punctual, and late replicas of the received m-sequence are obtained by tapping registers eight, nine, and ten, respectively. The punctual replica is fed to the punctual correlator to recover data. The early and late replicas are fed to their respective loop correlators.

Figure B.2 and B.3 show the early branch (correlator and data modifier) of the loop's correlator section. The late branch is identical. The inputs to this branch are the received m-sequence (demodulator output) and its early replica. The correlation operation is accomplished by multiplying these two inputs with an analog voltage multiplier (AVM, AD534) and then integrating this product with a low pass active filter. Attenuating these inputs prior to multiplication is necessary to prevent the AVM from saturating, and is achieved by cascading two inverting operational amplifiers (LM741). The variable DC voltage appearing at the differential inputs to the AVM perform a unipolar to bipolar conversion of the input signals. This conversion together with the variable DC output voltage adjustment ensures a positive or negative DC output whenever correlation occurs. The circuitry at the AVM's output multiplies that output by a factor of 100. This multiplication compensates for the 0.1 attenuation of the input signals and the 0.1 attenuation

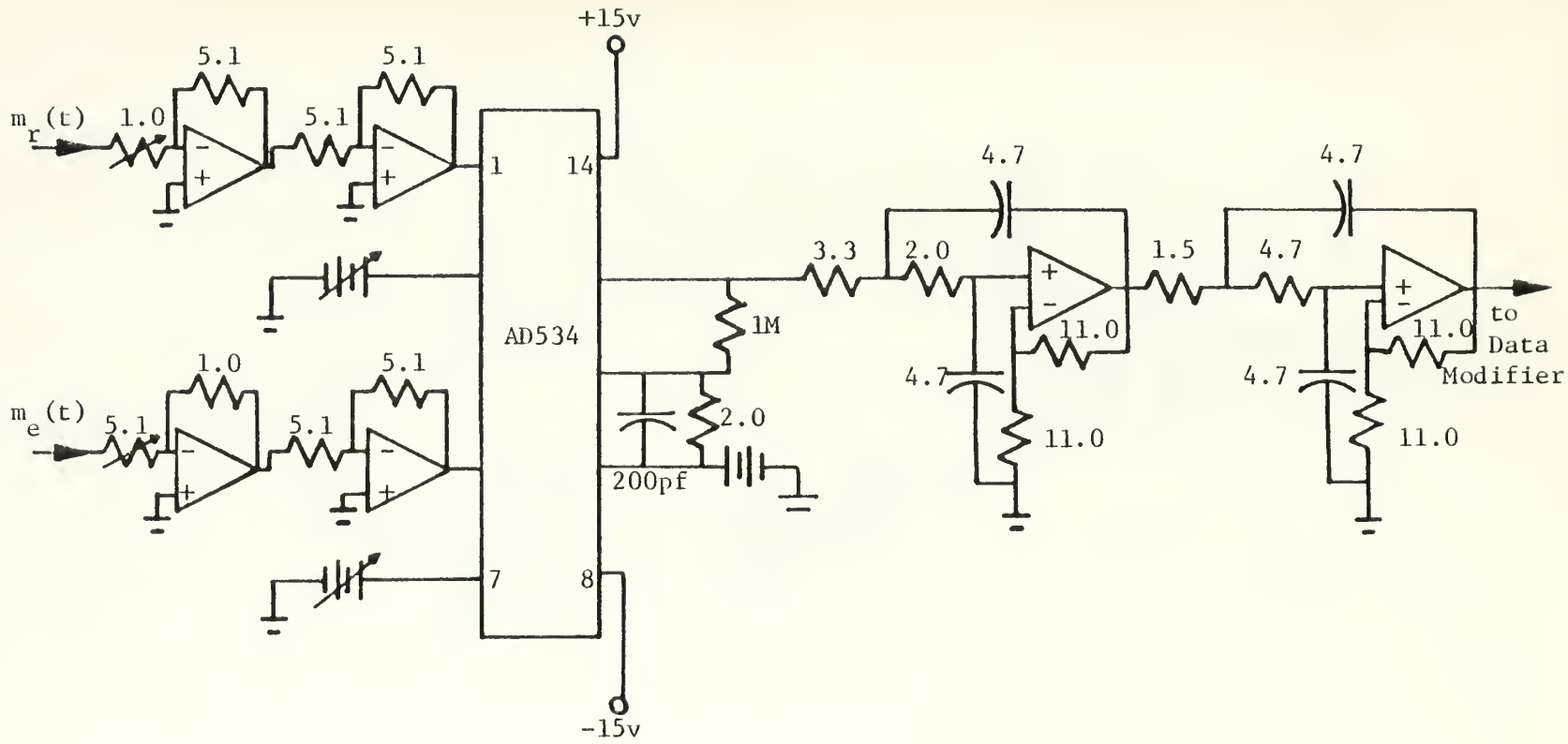


FIGURE B.2 EARLY CORRELATOR

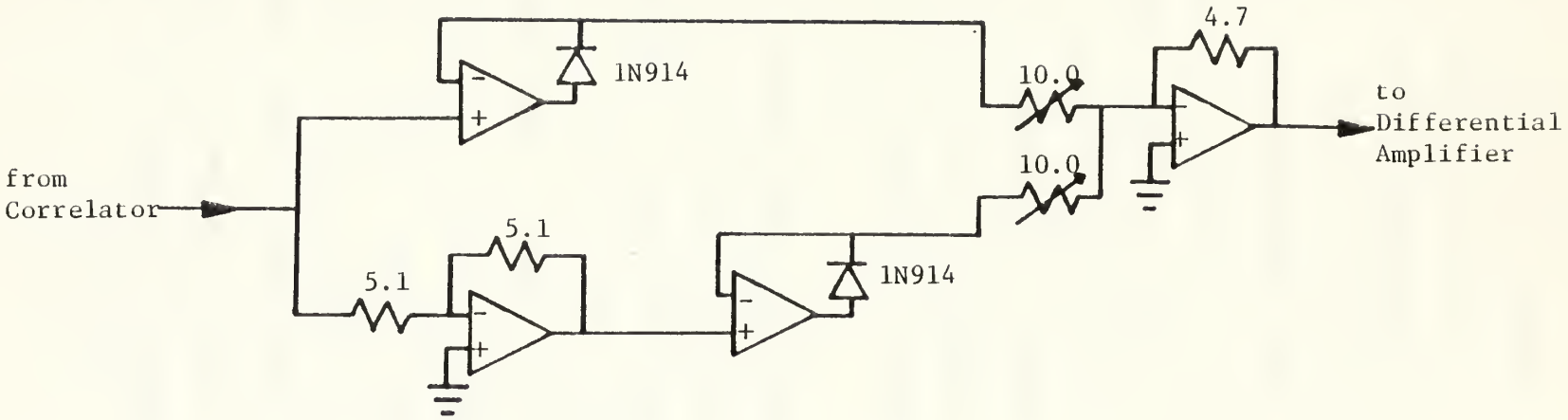


FIGURE B.3 DATA MODIFIER

factor inherent in the AVM, and provides a workable voltage level at the AVM's output. To complete the correlation operation, the AVM output is filtered by a lowpass fourth order active filter having a Butterworth frequency response characteristic. This filter is realized by cascading two lowpass second order filter sections. Each filter section is composed of an operational amplifier (LM741), capacitors, and resistors. A design frequency cutoff of 30 Hz and a gain of 4 is achieved by chosing the appropriate capacitor and resistor values. As explained in section III.A.2, this cutoff frequency is selected at a frequency greater than the data rate to allow the data modifier circuitry that follows to perform more effectively.

Figure B.3 shows the data modifier circuit. This circuit allows the loop to maintain synchronization while receiving data modulated m-sequences. Operational amplifiers (LM741) are used throughout to construct ideal diodes, inverters, and summers. As explained in section III.A.3, the ideal diode circuit eliminates the turn on voltage of the diode which, if allowed to remain, would disrupt the loop's operation. A silicon diode (1N914) is used in this application. The upper branch of the modifier circuit allows only positive voltages to pass. The lower branch inverts its input and then allows only positive voltages to pass. These voltages are summed by an operational amplifier which

inverts the voltage sum. Thus, the output of the modifier circuit is the negative value of whatever input voltage is applied.

The outputs of the loop's data modifier circuits are fed to the loop differential amplifier (LM741) as shown in Figure B.4. Here, the late minus early gate voltage is formed. Resistor values are chosen to provide a step down in voltage which is necessary to prevent the loop filter that follows from saturating.

In this loop design, the loop bandwidth is determined by the frequency response characteristics of the loop filter and the gain adjustment that follows. This experiment uses a lowpass fourth order active filter having a Chebychev frequency response characteristic. Two second order filter sections are cascaded to form this filter. Each filter section is composed of an operational amplifier and appropriately valued capacitors and resistors. The design cutoff frequency is varied during this experiment (2.3, 4.0, 6.3 Hz) by changing the filter's four equi-value capacitors. Reference 5 outlines the design for all filters used throughout the loop. The loop gain adjustment that follows forms the final version of the loop error voltage $v_d(t)$. Two inverting operational amplifiers are cascaded to form this circuit. Gain adjustments are made by varying the two potentiometers as shown in Figure B.4.

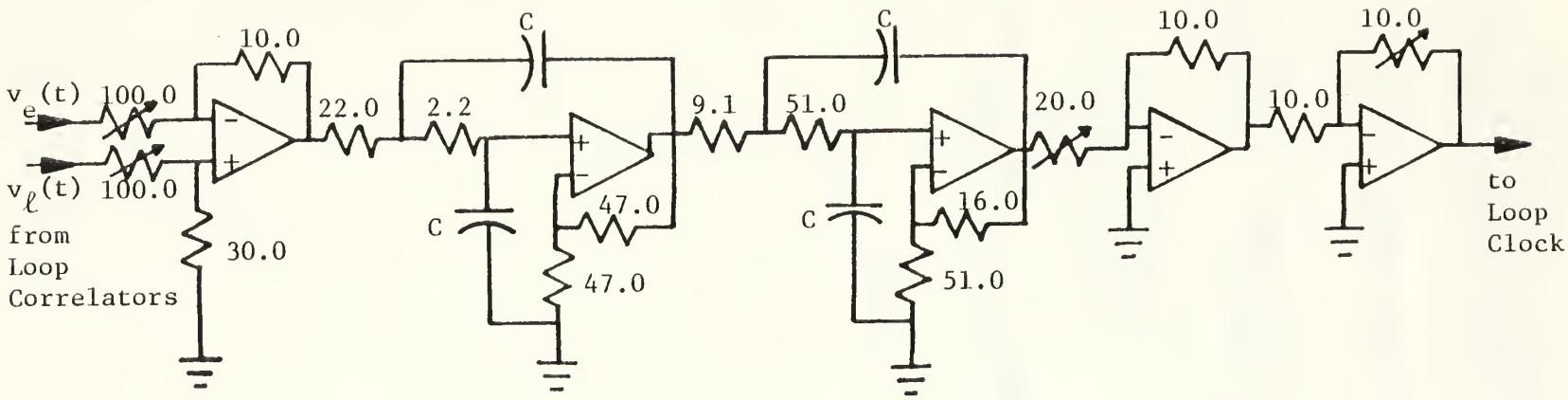


FIGURE B.4 LOOP DIFFERENTIAL AMPLIFIER, FILTER, AND GAIN

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